

# Compal Confidential

## PLA00 LA6951P Schematics Document

### Intel Sandy Bridge Processor with DDRIII + Cougar Point

### AIO M/B

2011-02-24

REV: 1 . A

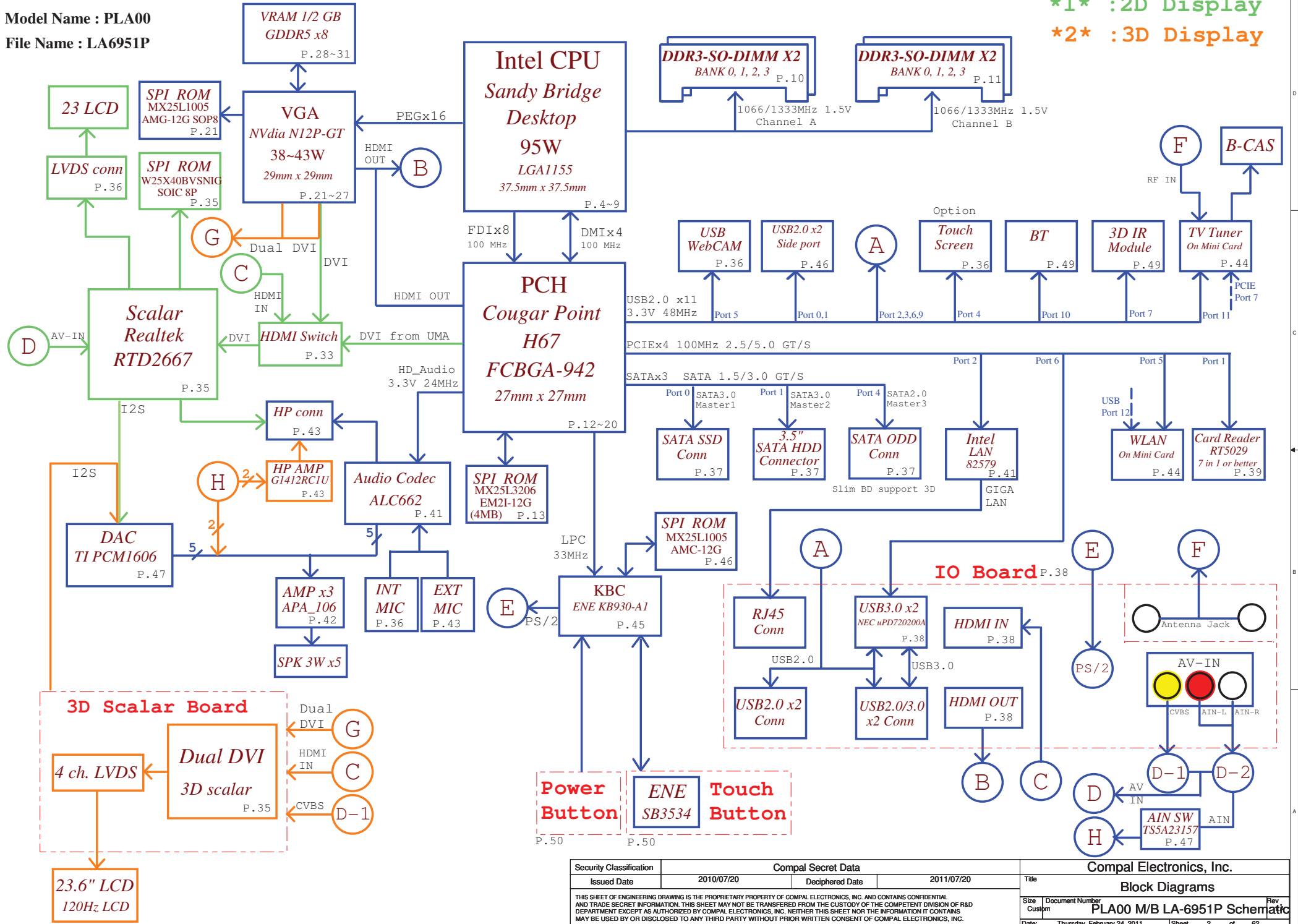
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Model Name : PLA00

File Name : LA6951P

\*1\* :2D Display  
\*2\* :3D Display



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## Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

## SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@ (VRAM:Hynix)
0	1	0	DIS@ (VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

## BOARD ID Table

Board ID	Ra/Rb	Vad-bid
AV SKU	R442 100K	3.3V
NON AV SKU	R445 0 ohm	0 V

## USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
7		3D IR	
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(WLAN)
	UHCI6	12	Mini Car(TV Tuner
		13	

## BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
CRT	CRT@
PCML606	1606@
Samsung VRAM (1G)	x76_SAM@
Hynix VRAM (1G)	x76_HYN@
Samsung VRAM (2G)	x76_SAM2G@
Hynix VRAM (2G)	x76_HYN2G@
AV-IN SKU	AV@
No AV-IN SKU	NON_AV@

## EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

## PCH SM Bus address

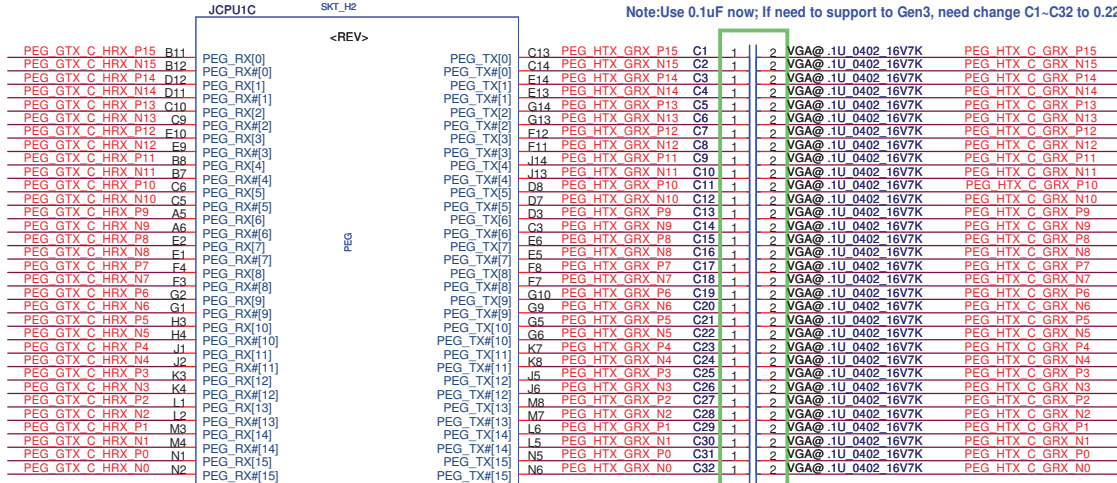
Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

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DMI\_PTX\_HRX\_N[0..3] <14>  
DMI\_PTX\_HRX\_P[0..3] <14>  
DMI\_HTX\_PRX\_N[0..3] <14>  
DMI\_HTX\_PRX\_P[0..3] <14>

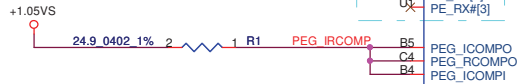
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PEG GTX\_C\_HRX\_N[0..15] <22>  
PEG HTX\_C\_GRX\_P[0..15] <22>  
PEG HTX\_C\_GRX\_N[0..15] <22>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

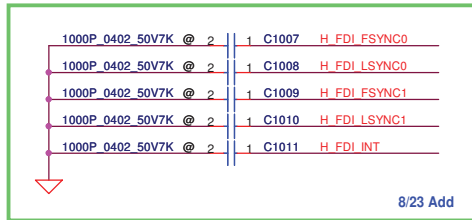


DMI\_PTX\_HRX\_P0 W5  
DMI\_PTX\_HRX\_N0 W4  
DMI\_PTX\_HRX\_P1 V3  
DMI\_PTX\_HRX\_N1 V4  
DMI\_PTX\_HRX\_P2 V3  
DMI\_PTX\_HRX\_N2 Y4  
DMI\_PTX\_HRX\_P3 AA4  
DMI\_PTX\_HRX\_N3 AA5  
DMI\_RX[0] W5  
DMI\_RX[0] W4  
DMI\_RX[0] V3  
DMI\_RX[0] V4  
DMI\_RX[0] V3  
DMI\_RX[0] Y4  
DMI\_RX[0] AA4  
DMI\_RX[0] AA5  
DMI\_TX[0] W5  
DMI\_TX[0] W4  
DMI\_TX[0] V3  
DMI\_TX[0] V4  
DMI\_TX[0] V3  
DMI\_TX[0] Y4  
DMI\_TX[0] AA4  
DMI\_TX[0] AA5

7/20 PE\_RX[0~3]/PE\_TX[0~3] only use on Workstation.



PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - ;Width/Space= (4 mils/15mils)  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - Width/Space (12 mils/15mils)



7/20 PE\_TX[0~3]/PE\_TX[0~3] only use on Workstation.

<16> H\_FDI\_FSYNC0

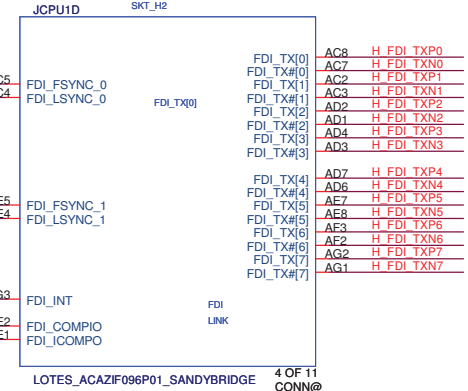
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<16> H\_FDI\_FSYNC1

<16> H\_FDI\_LSYNC1

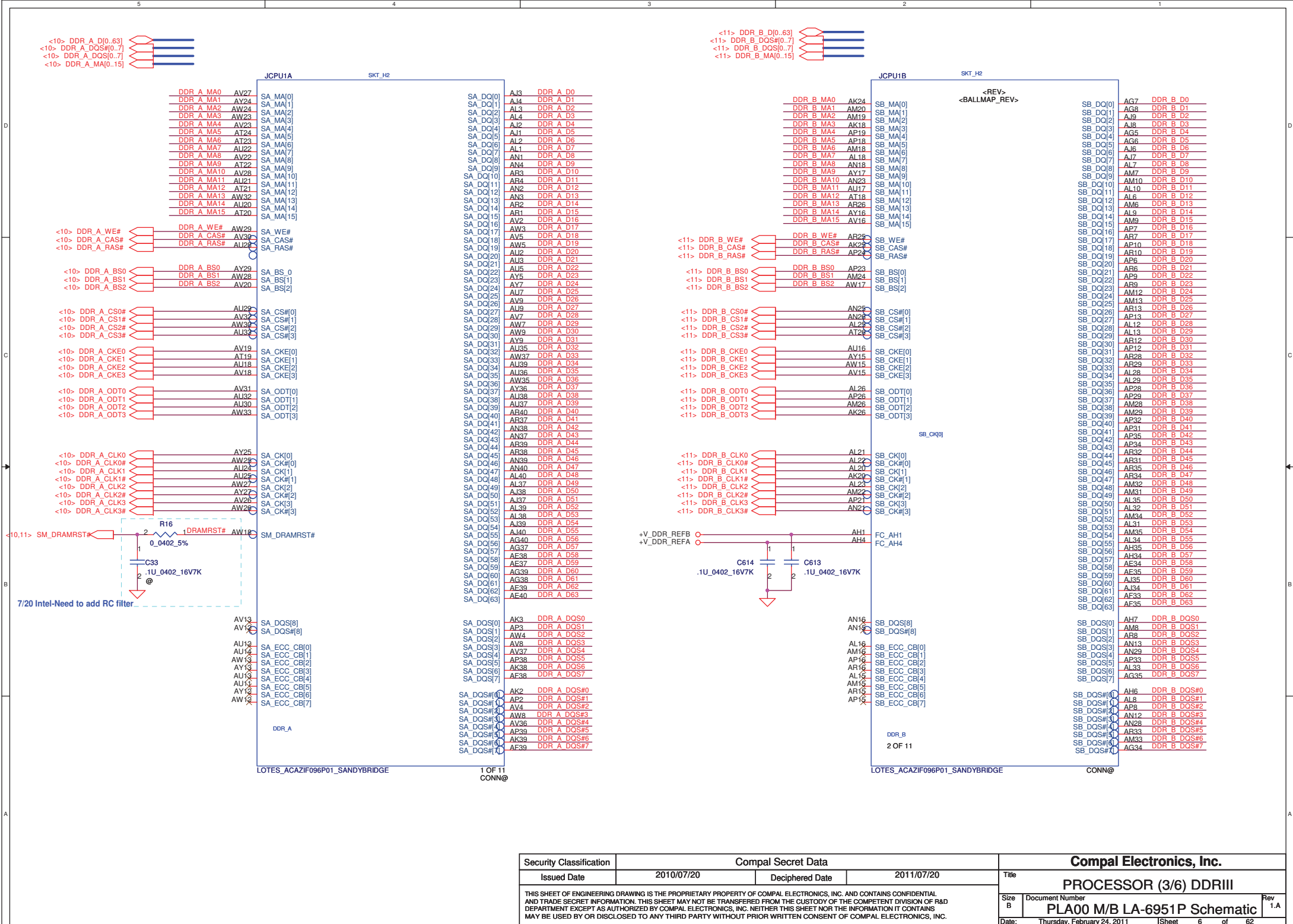
<16> H\_FDI\_INT

H\_FDI\_TXN[0..7] <16>  
H\_FDI\_TXP[0..7] <16>

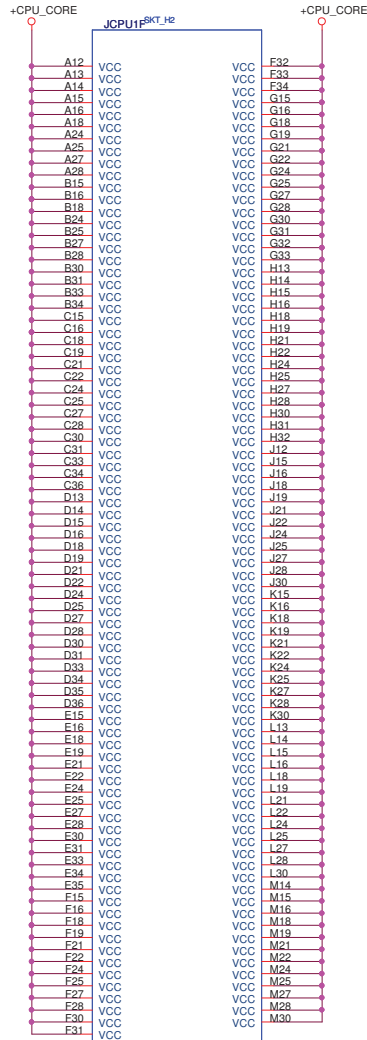


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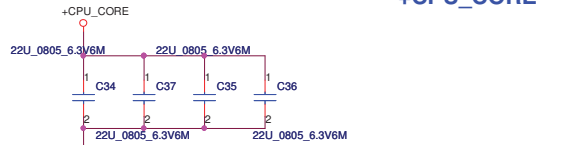


# +CPU\_CORE:112A

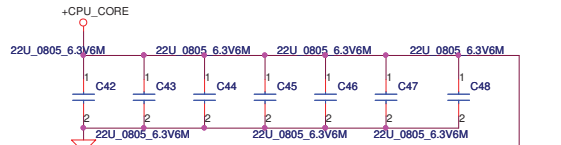


CPU POWER  
6 OF 11  
LOTES\_ACAZIF096P01\_SANDYBRIDGE  
CONN@

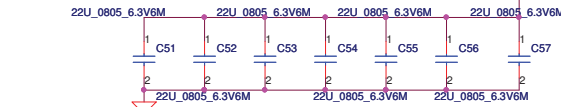
## +CPU\_CORE



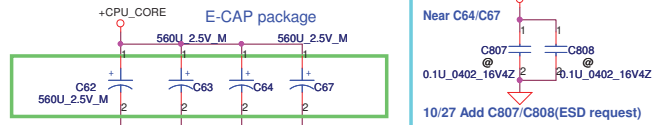
(Place these capacitors inside CPU socket cavity, top layer)



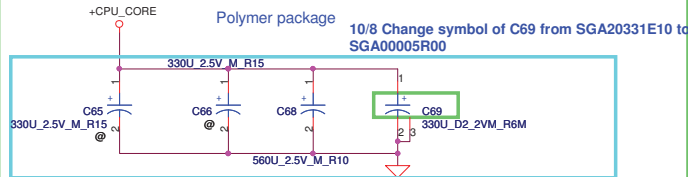
(Place these capacitors under CPU socket, Bottom layer)



(Place these capacitors under CPU socket, Bottom layer)

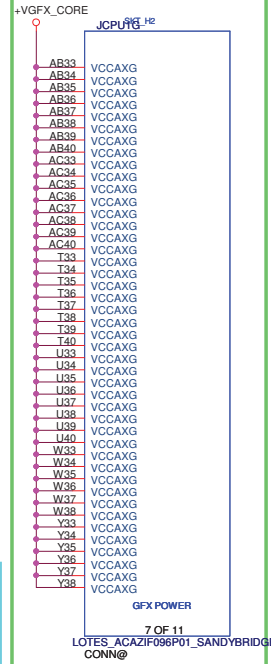


8/24 Change symbol of C62-C63 from SF000001P00 to SF000001K00  
(Place C62-C64 capacitors under CPU socket, Top layer)

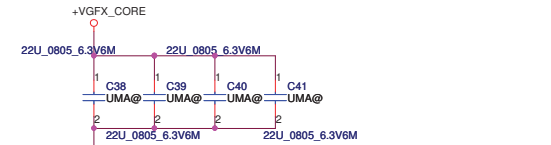


10/23 Change symbol of C65/C66/C68 from SGA20331E10 to SF000002M00  
(Place C65-C69 capacitors under CPU socket, Bottom layer)  
11/2 Change PN of C68 from SF000002M00 to SF000001K00

# +VGFX\_CORE:35A



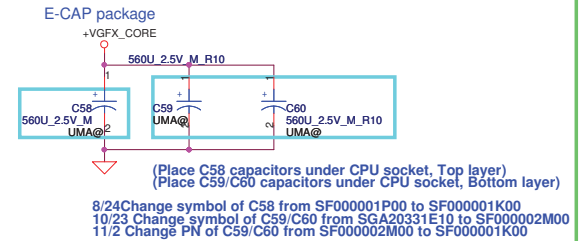
## +VGFX\_CORE



(Place these capacitors inside CPU socket cavity, top layer)

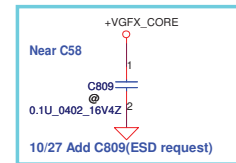


(Place these capacitors under CPU socket, Bottom layer)



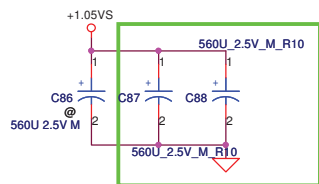
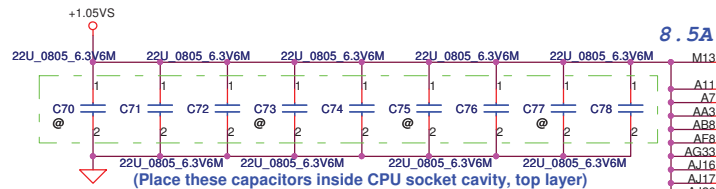
(Place C58 capacitors under CPU socket, Top layer)  
(Place C59/C60 capacitors under CPU socket, Bottom layer)

8/24 Change symbol of C58 from SF000001P00 to SF000001K00  
10/23 Change symbol of C59/C60 from SGA20331E10 to SF000002M00  
11/2 Change PN of C59/C60 from SF000002M00 to SF000001K00



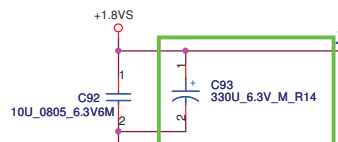
10/27 Add C809(ESD request)

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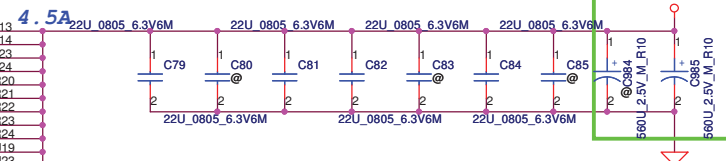
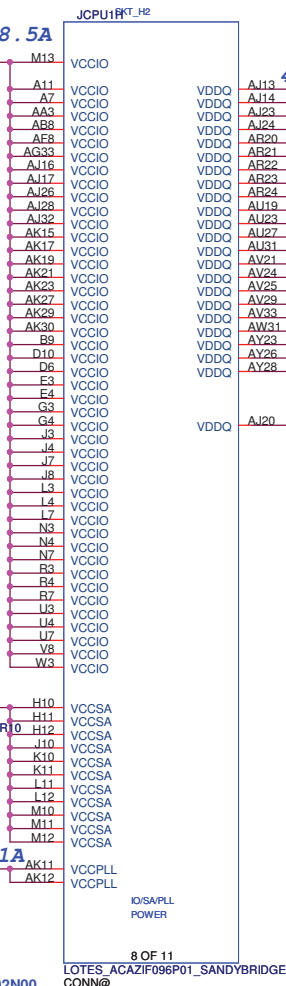


11/2 Change PN of C87/C88 from SF000001P00 to SF000001K00

11/4 Change PN of C91 from SF000001P00 to SF000001K00

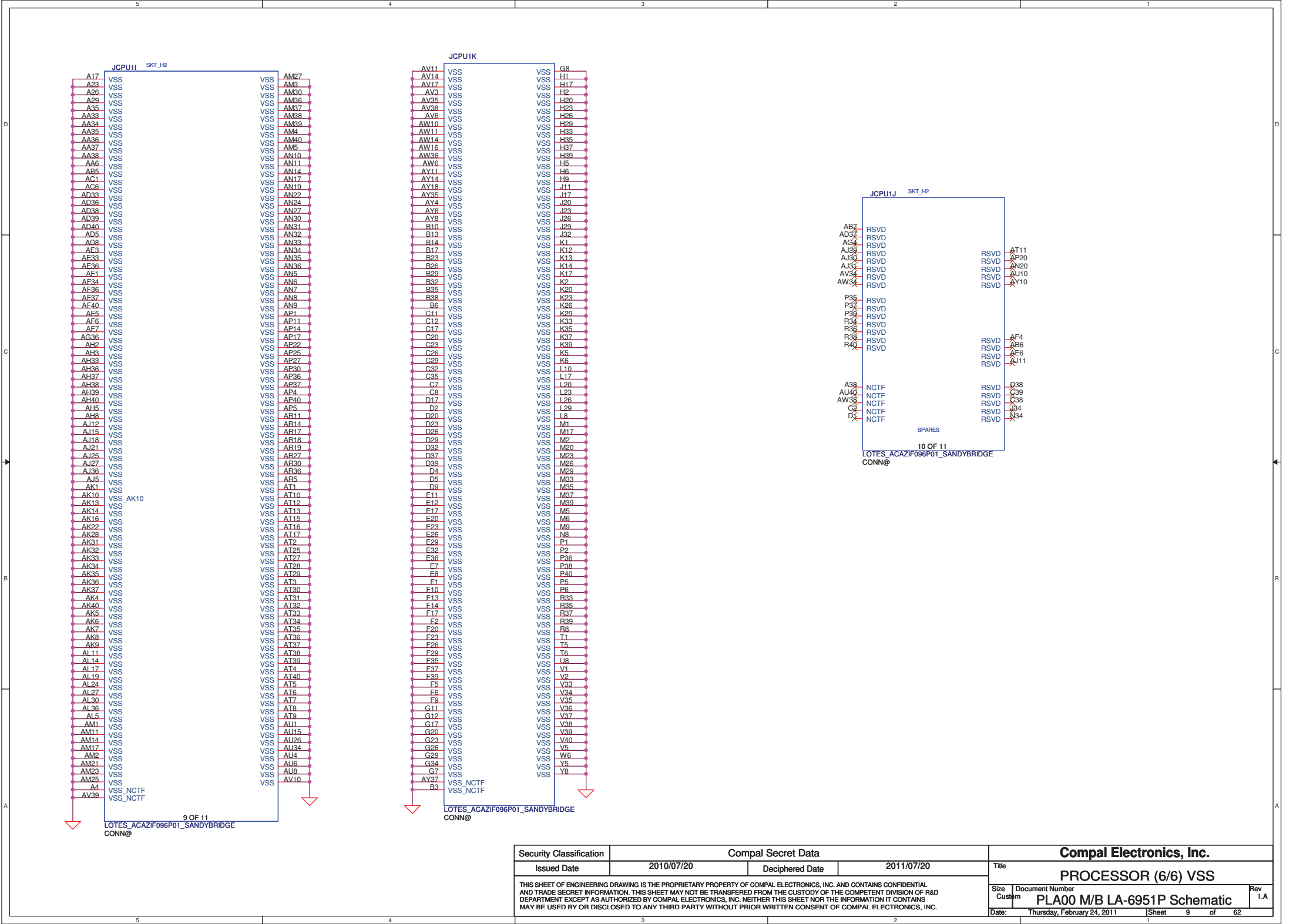


10/23 Change symbol of C93 from SGA00000Y80 to SF000002N00  
11/4 Change PN of C93 from SF000002N00 to SF000001G00

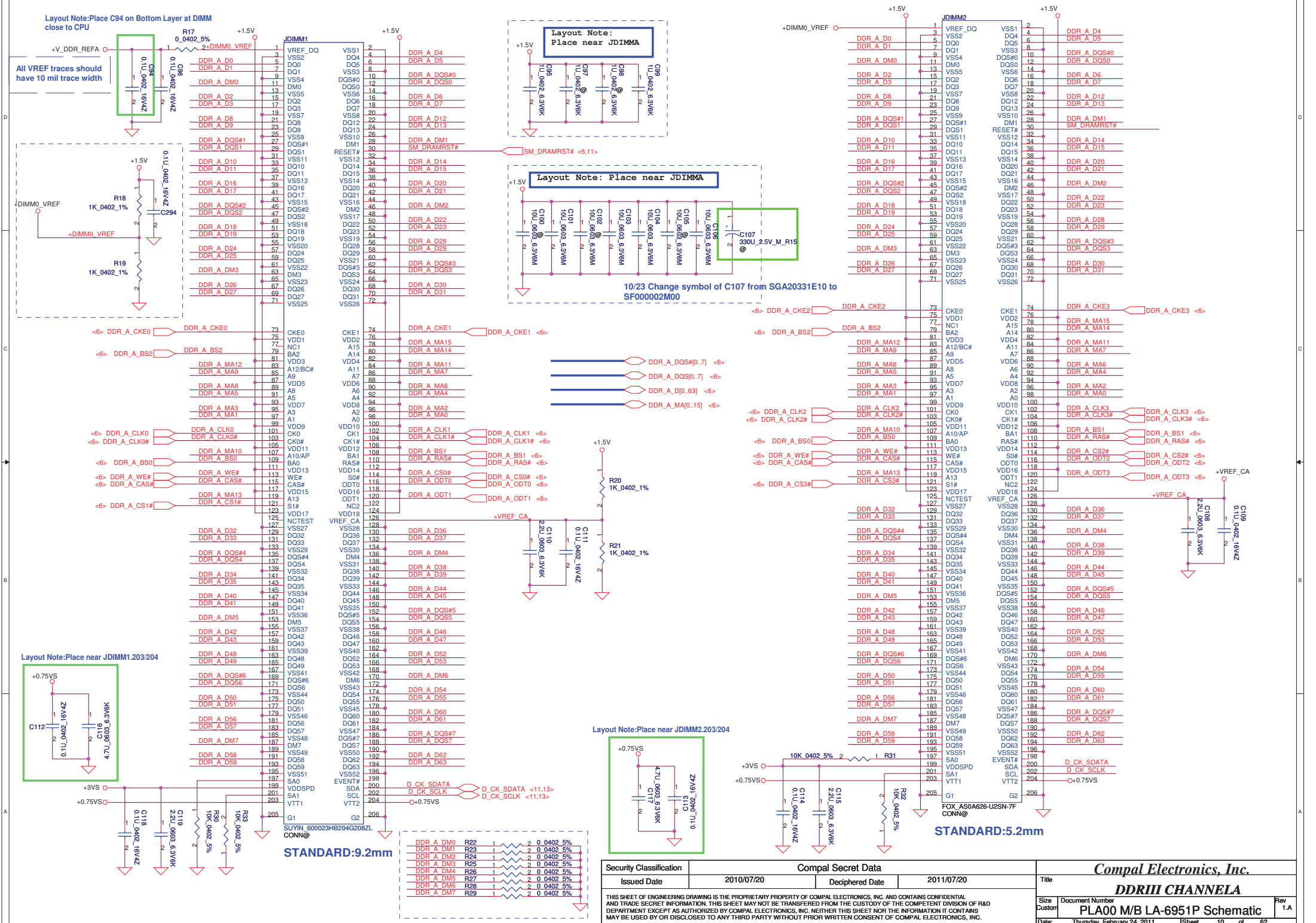


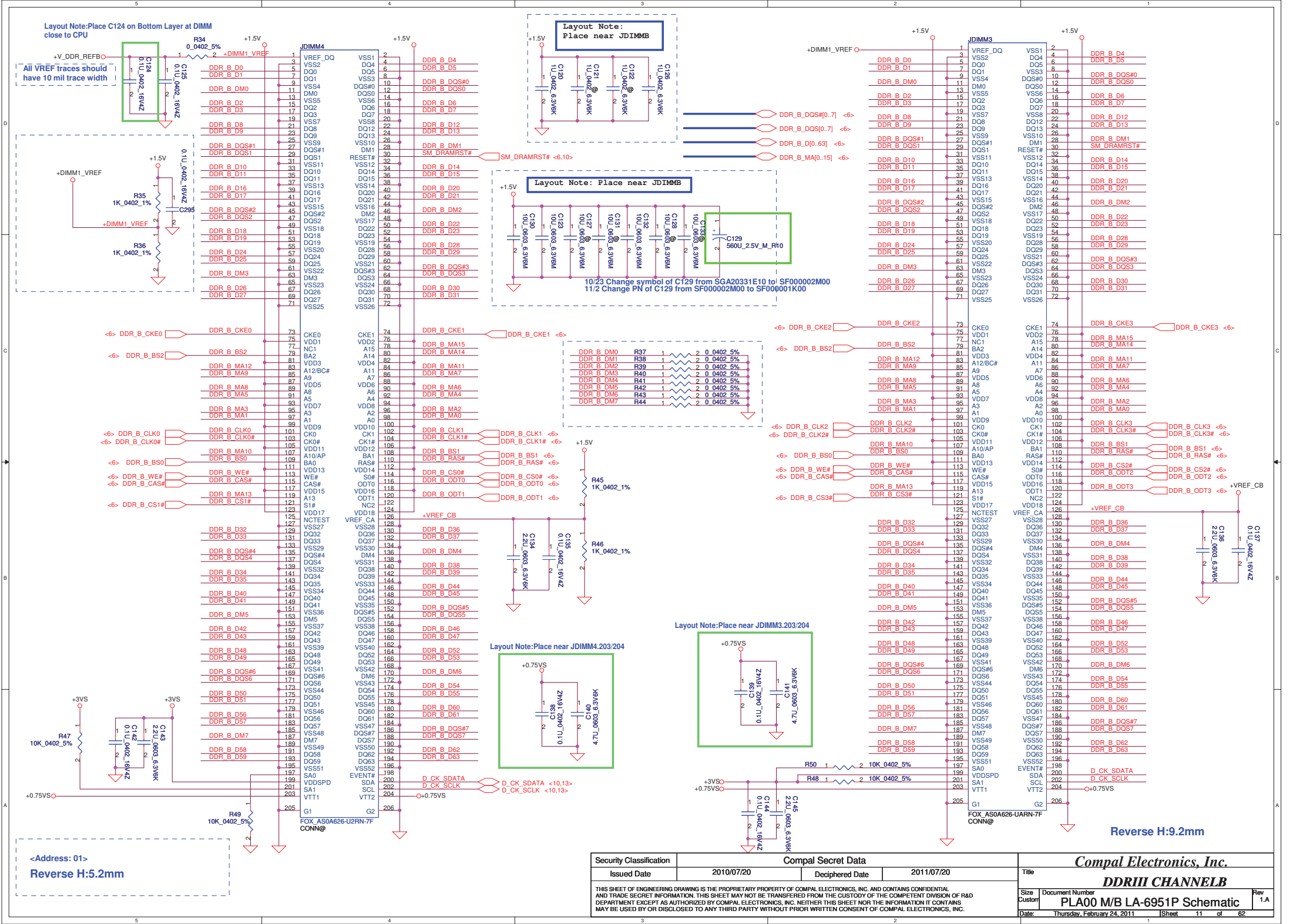
11/2 Change PN of C984/C985 from SF000002000 to SF000001K00

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<41> HDA\_BITCLK\_AUDIO <R69> 1 2 HDA\_BITCLK\_PCH 33\_0402\_5%

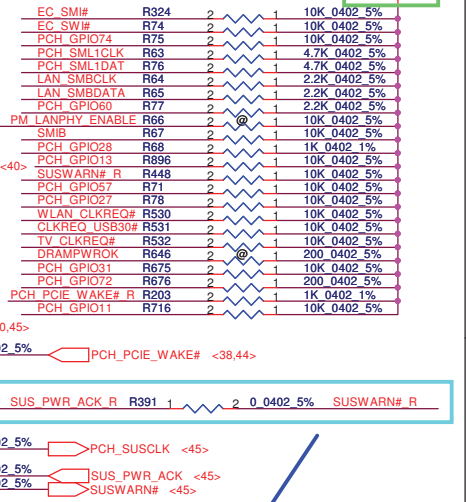
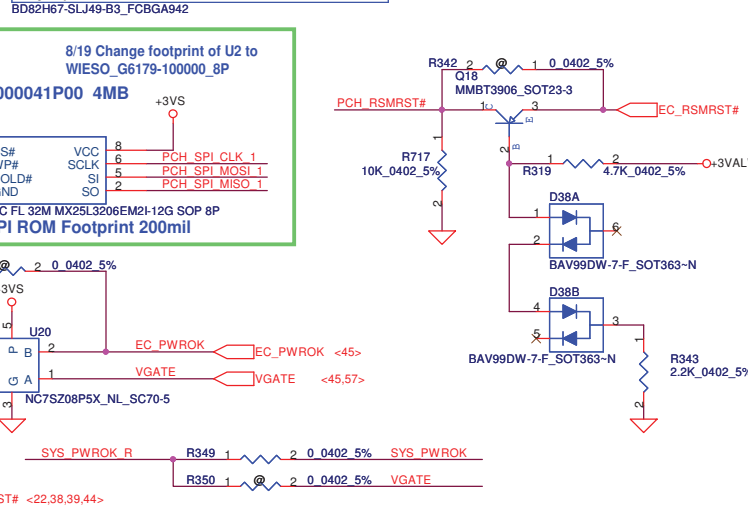
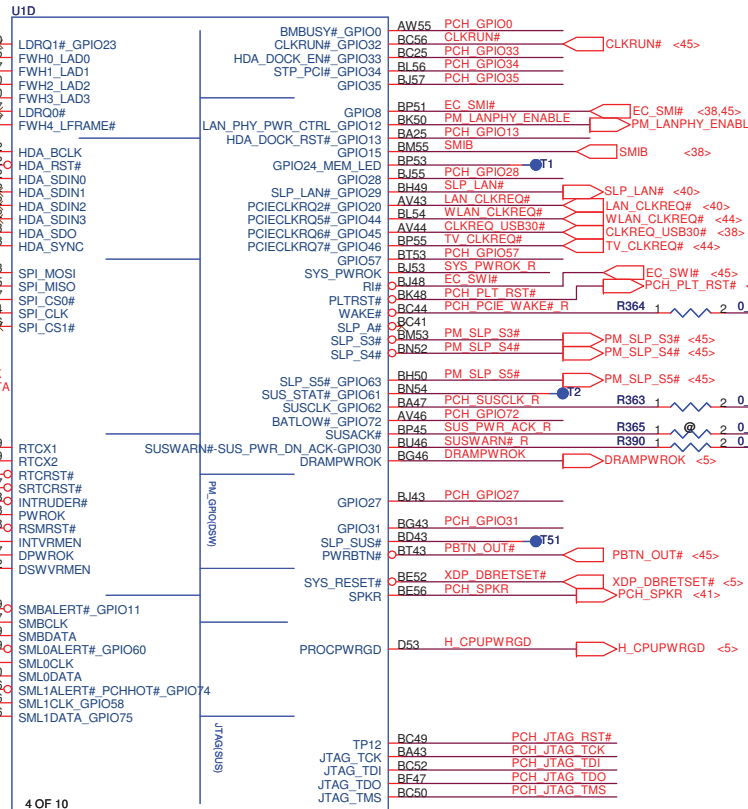
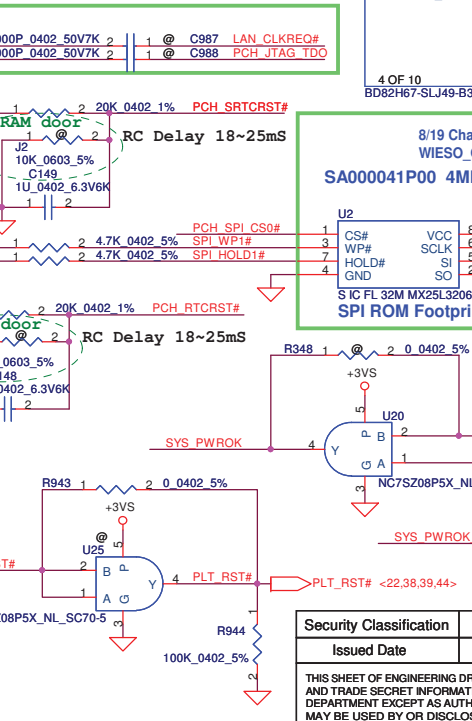
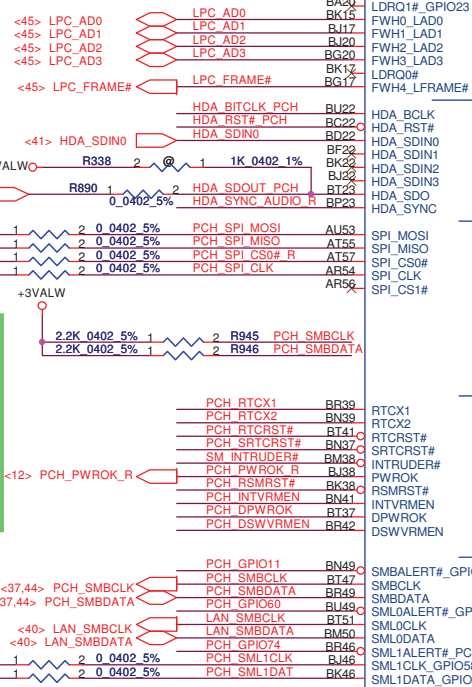
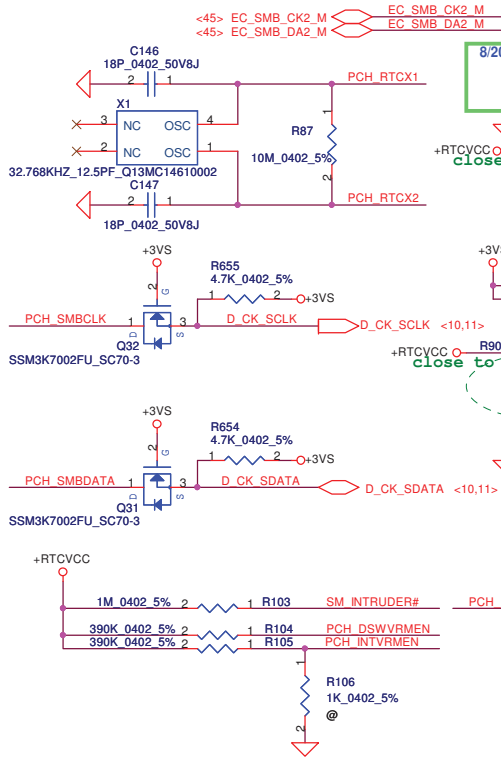
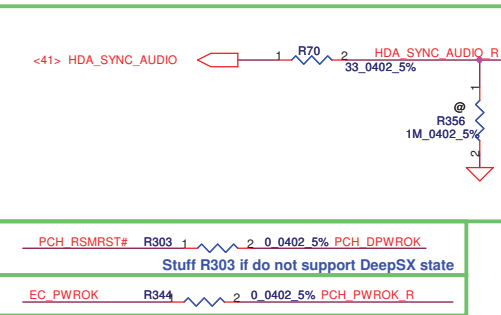
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<41> HDA\_SDOUT\_AUDIO <R73> 1 2 HDA\_SDOUT\_PCH 33\_0402\_5%

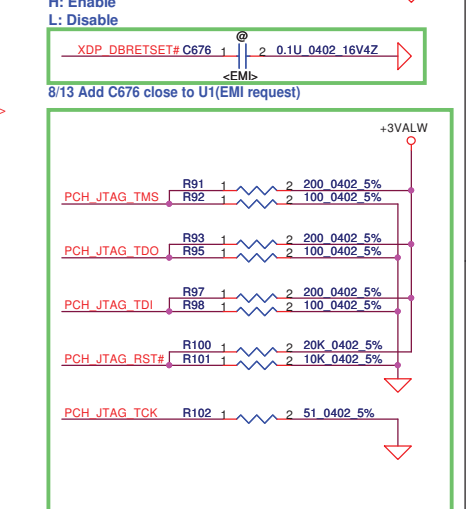
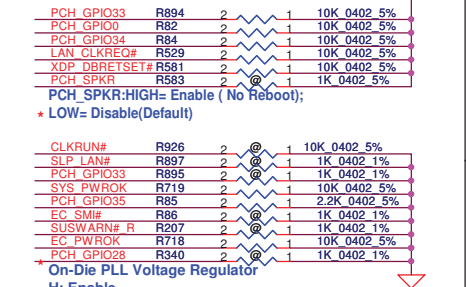
ME debug mode,  
this signal has a weak internal pull down

- ★ Low = Disable (default)
- High = Enable (flash descriptor security override)

This signal has a weak internal pull down  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V  
★Need to pull high for Huron River platform

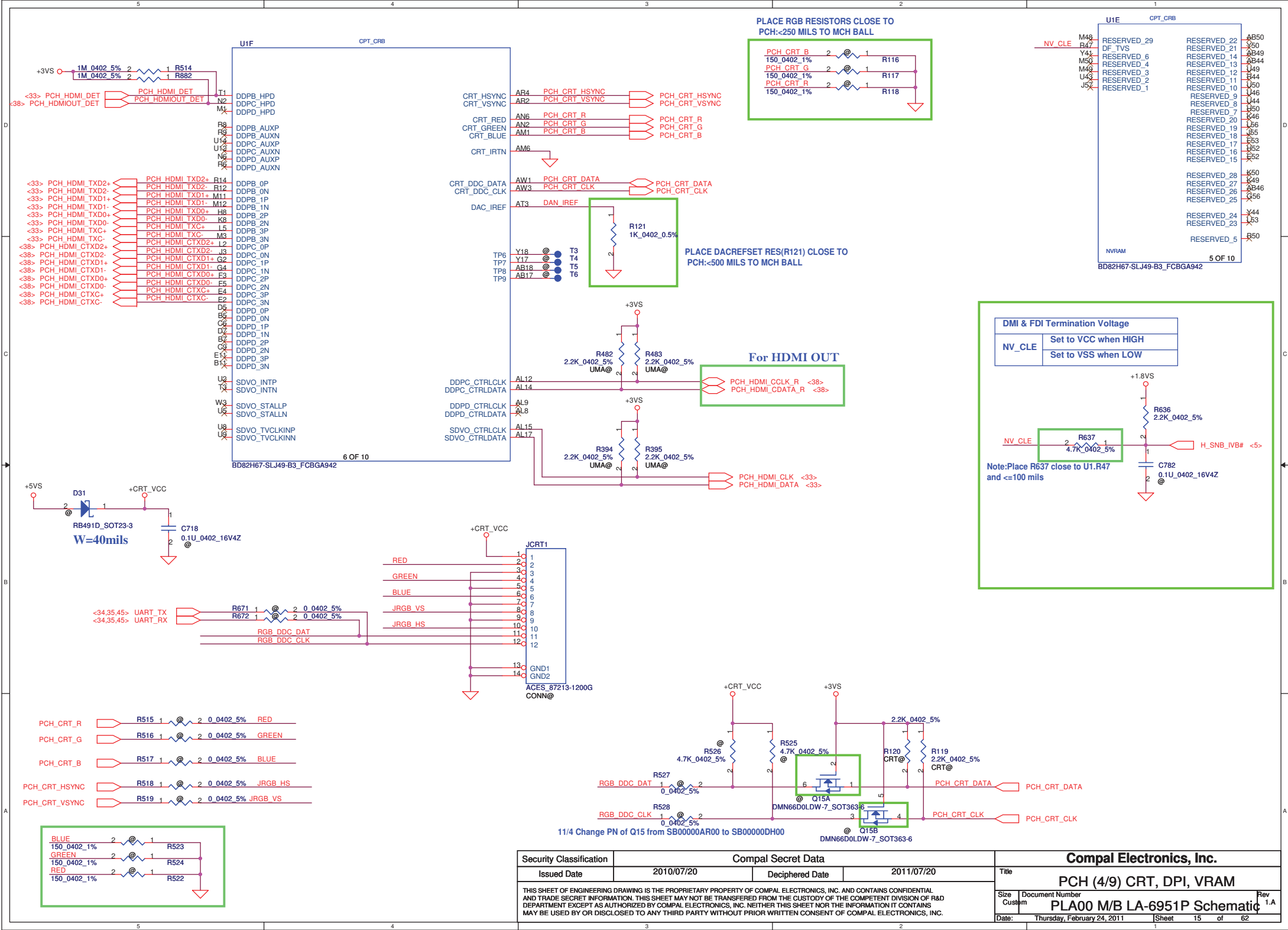


Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit

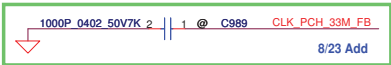
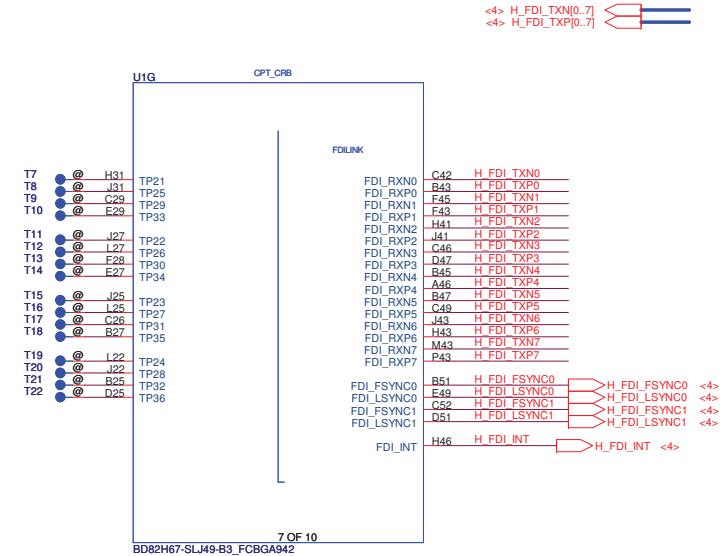
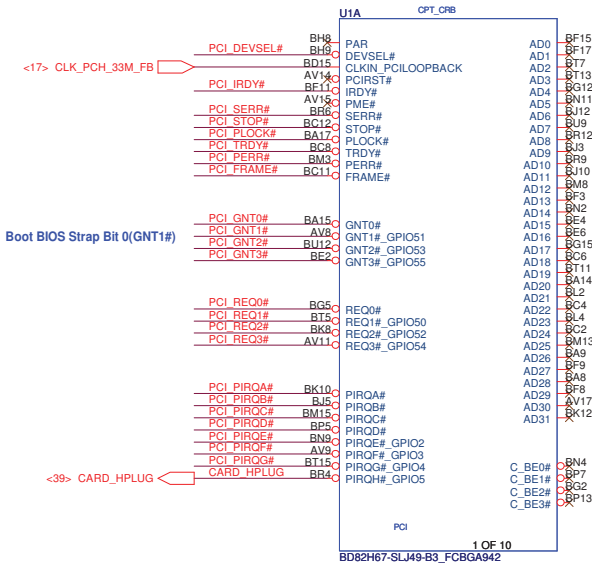
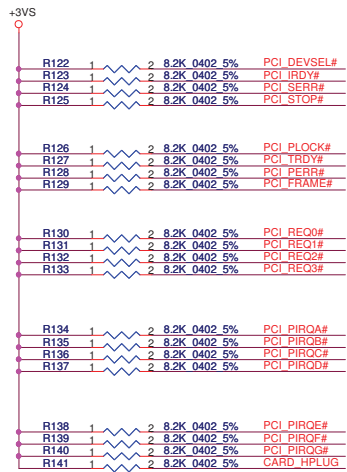


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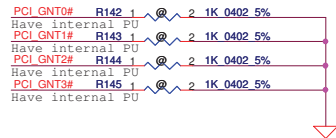


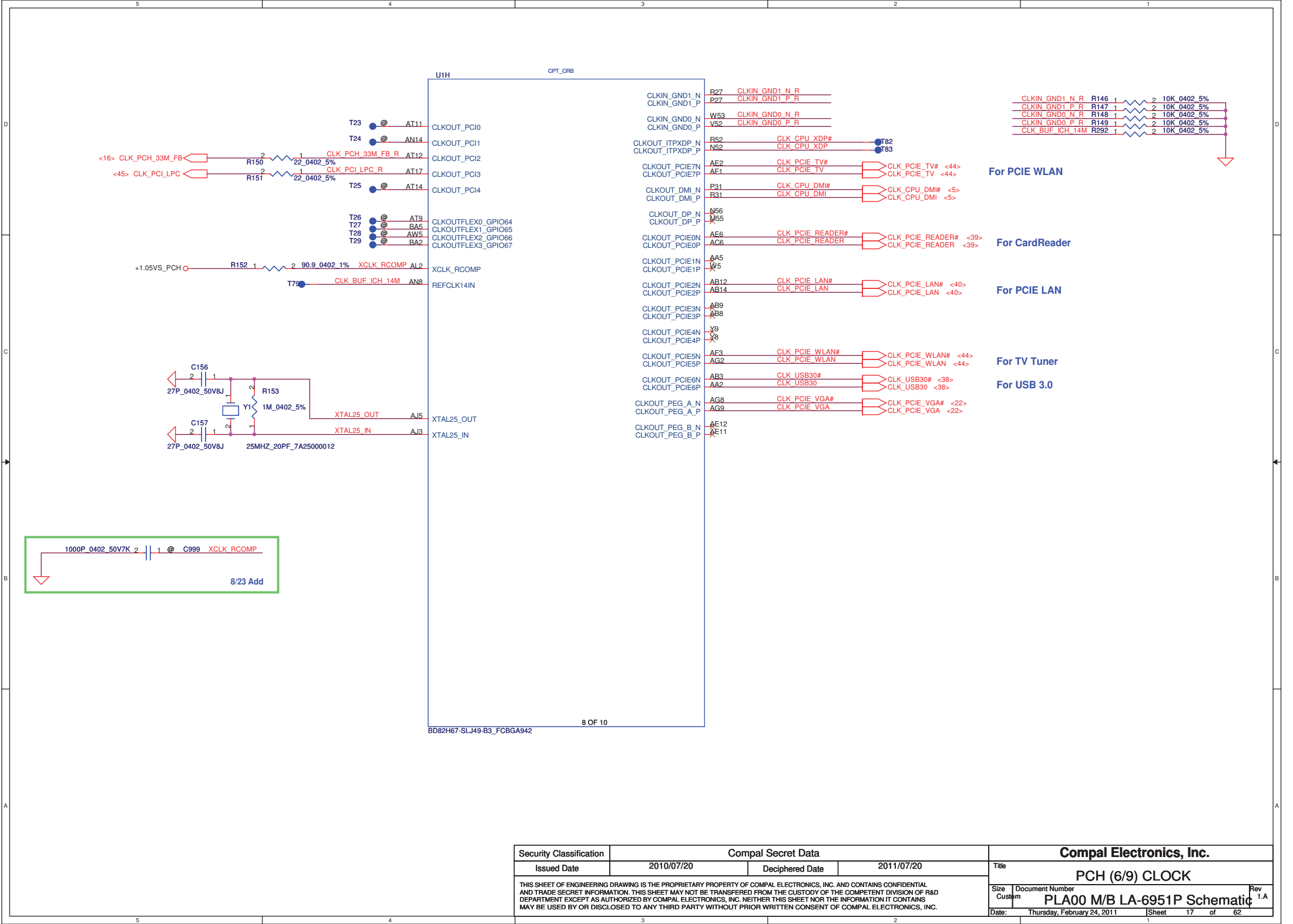


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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	15	of	62

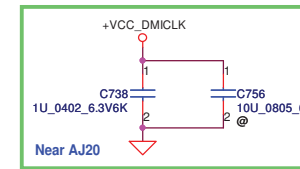
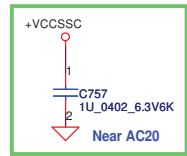
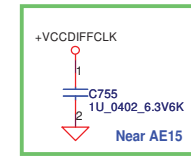
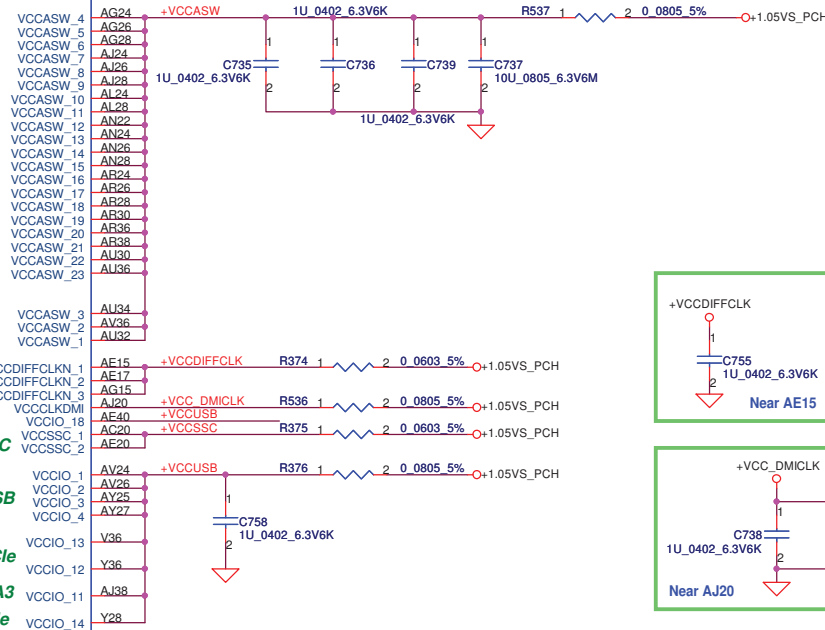
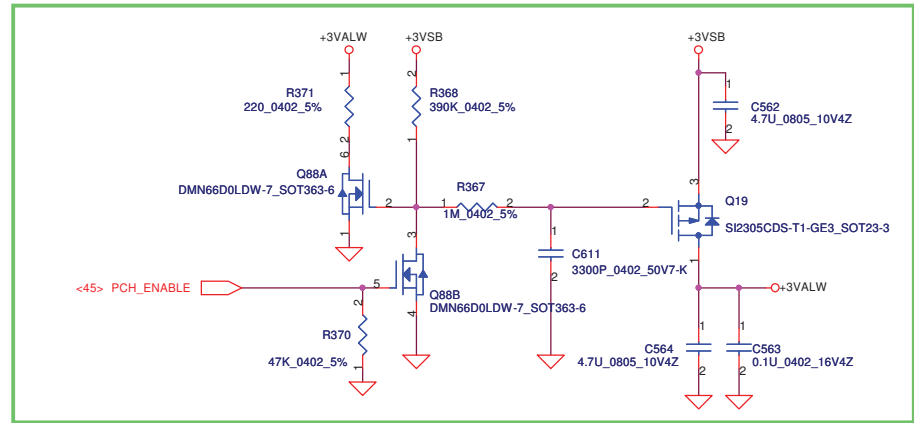
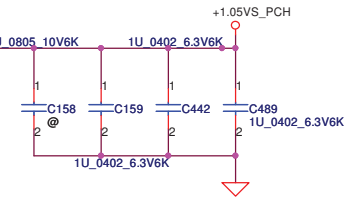
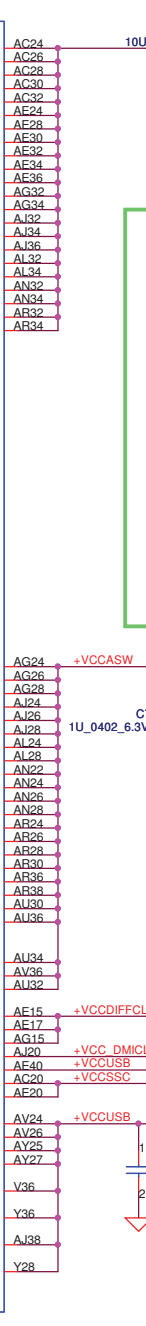
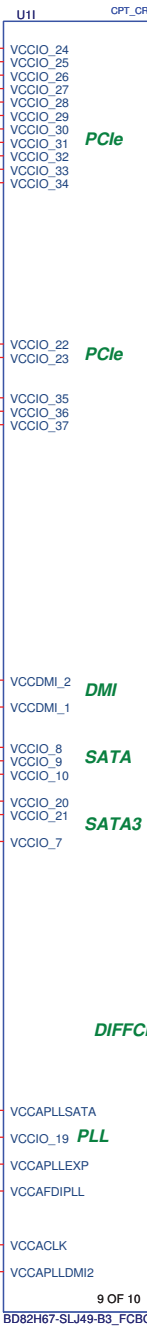
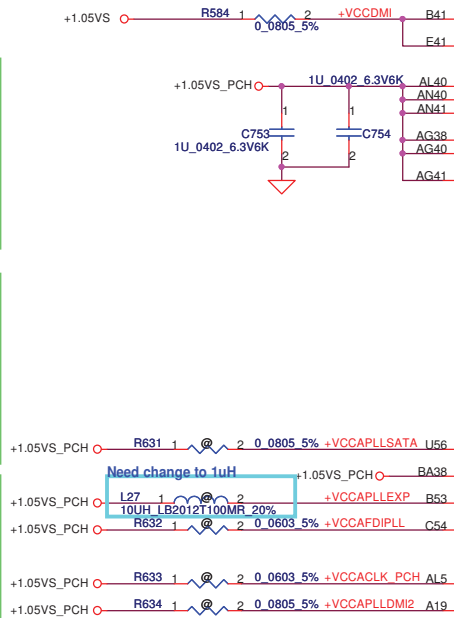
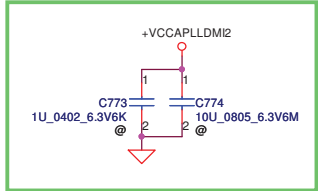
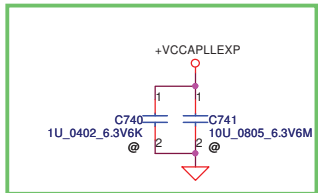
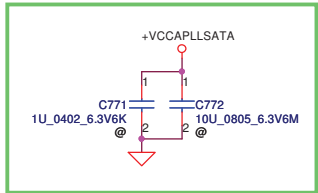
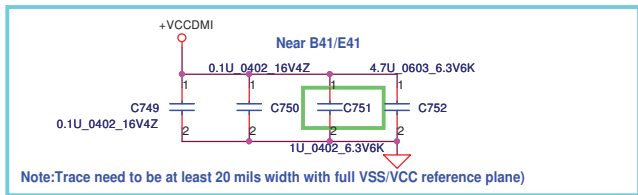
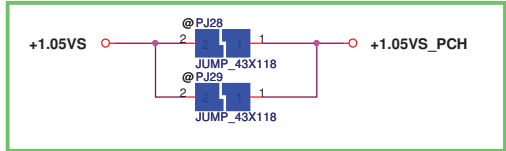
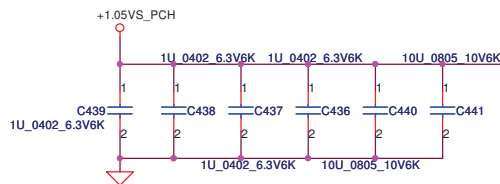


Boot BIOS Strap		
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0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

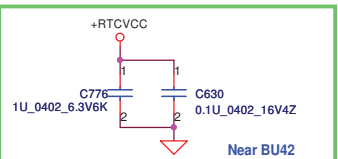
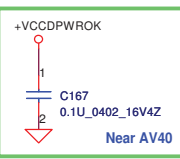
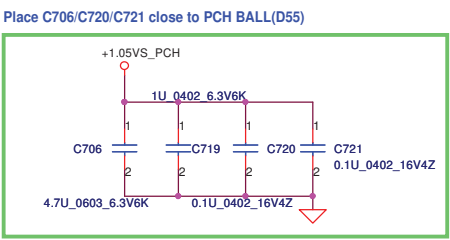
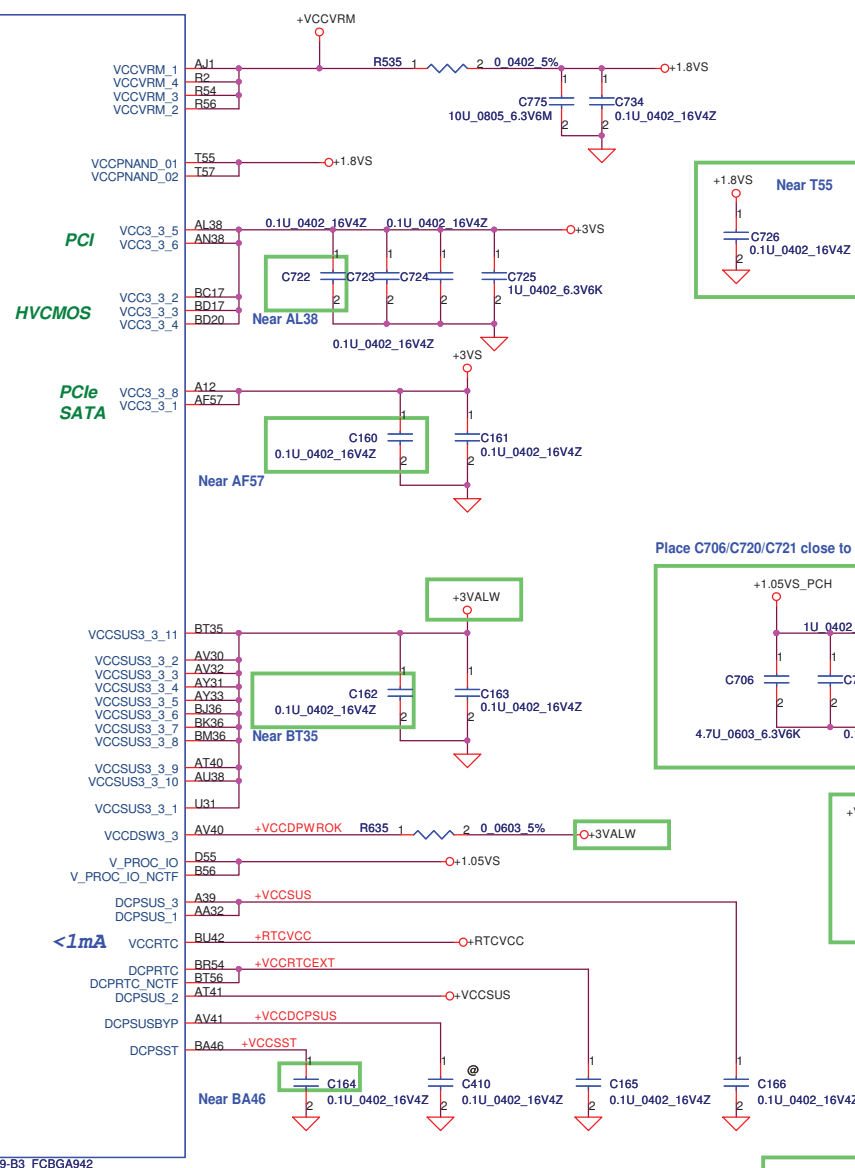
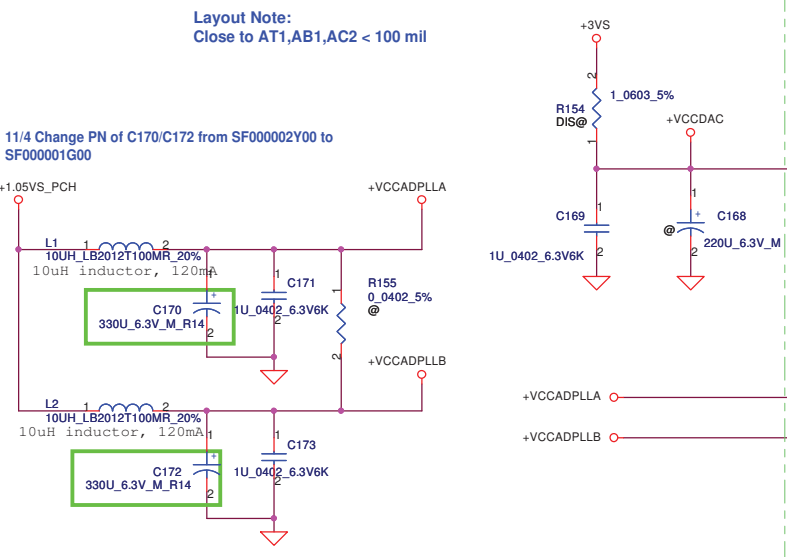
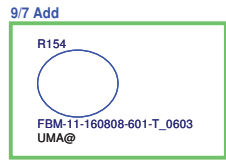
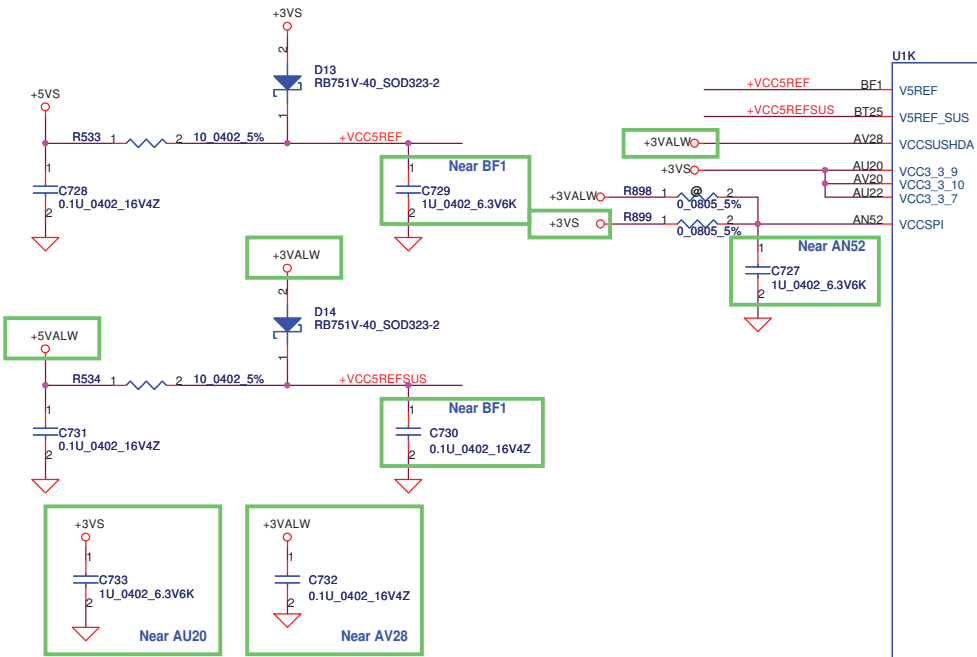




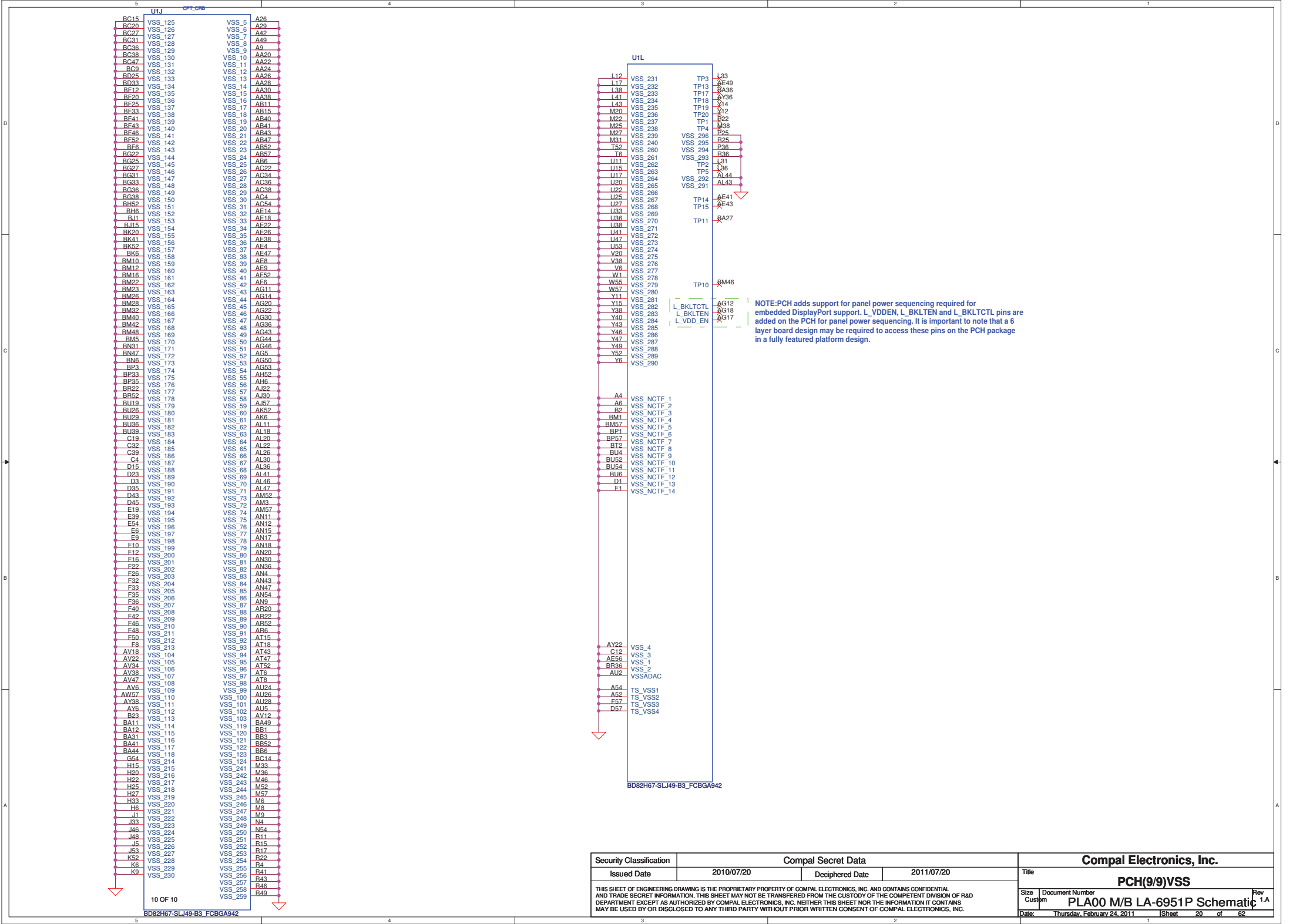
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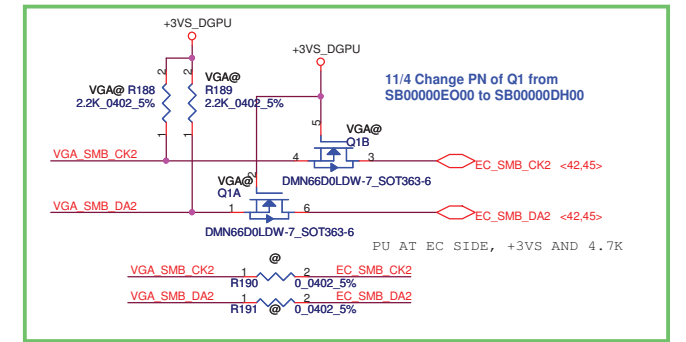
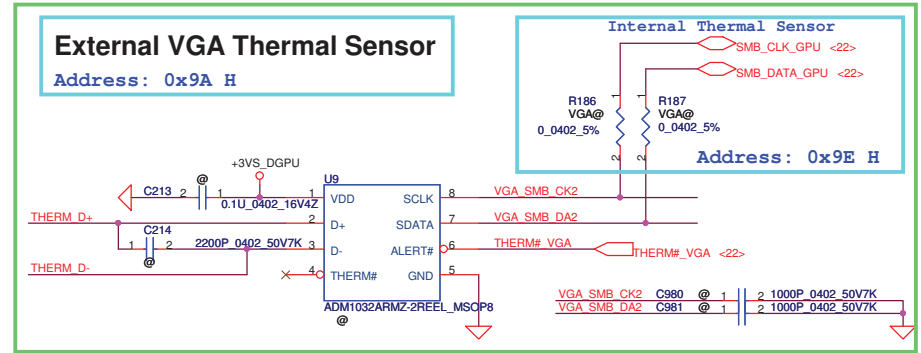
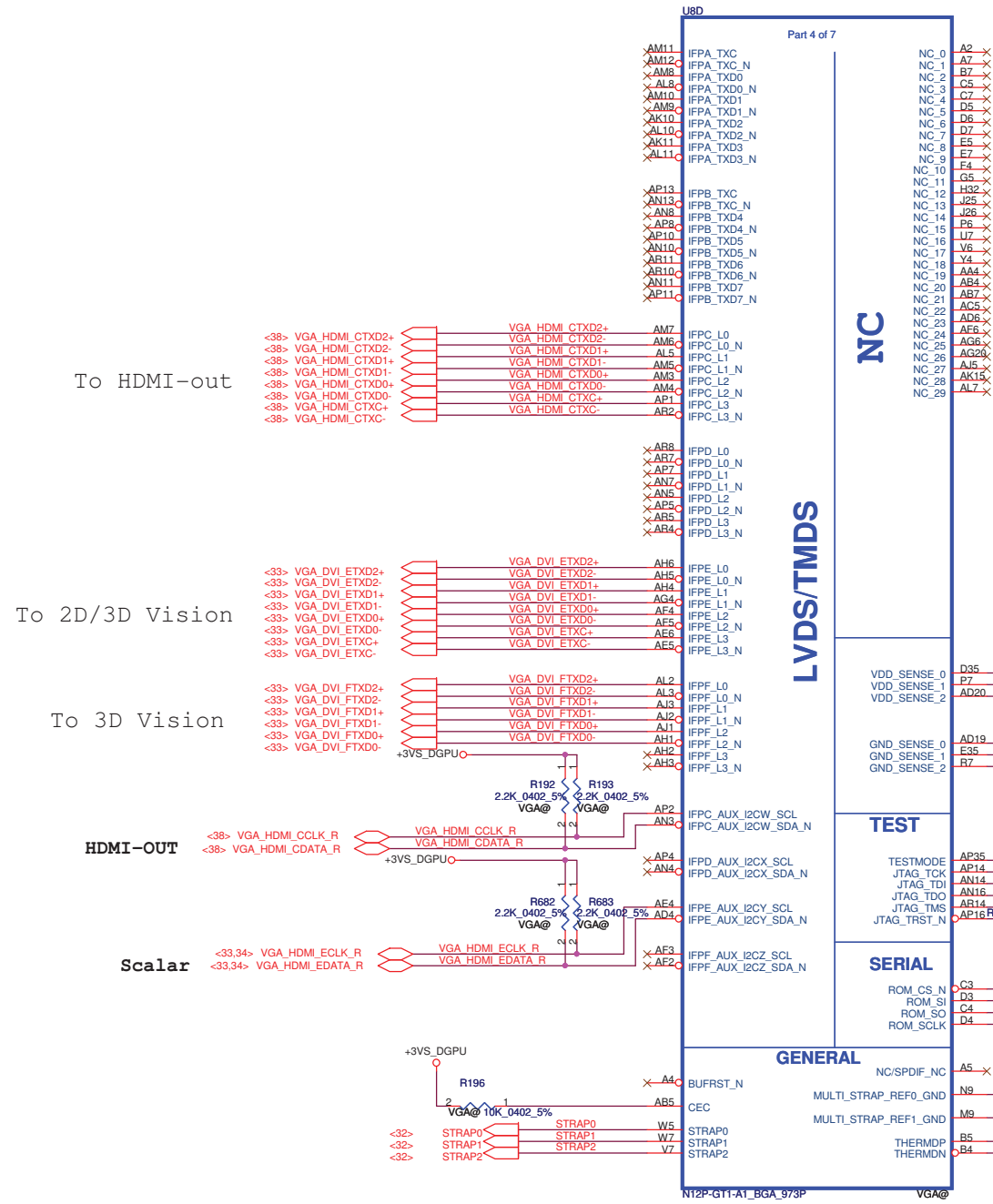
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<div><div><div><div><div>K52</div><div>VSS_228</div></div><div><div>K6</div><div>VSS_229</div></div><div><div>K9</div><div>VSS_230</div></div></div><div>10 OF 10</div><div>BD82H67-SLJ49-B3_FCBGA942</div></div></div>				<table><tr><th colspan="2">Security Classification</th><th colspan="2">Compal Secret Data</th></tr><tr><td>Issued Date</td><td>2010/07/20</td><td>Deciphered Date</td><td>2011/07/20</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td></tr></table>				Security Classification		Compal Secret Data		Issued Date	2010/07/20	Deciphered Date	2011/07/20	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<table><tr><th colspan="4">Compal Electronics, Inc.</th></tr><tr><td colspan="4">Title</td></tr><tr><td colspan="4">PCH(9/9)VSS</td></tr><tr><td>Size</td><td>Document Number</td><td colspan="2">Rev</td></tr><tr><td>Custom</td><td>PLA00 M/B LA-6951P Schematic</td><td colspan="2">1.A</td></tr><tr><td>Date:</td><td>Thursday, February 24, 2011</td><td>Sheet</td><td>20 of 62</td></tr></table>				Compal Electronics, Inc.				Title				PCH(9/9)VSS				Size	Document Number	Rev		Custom	PLA00 M/B LA-6951P Schematic	1.A		Date:	Thursday, February 24, 2011	Sheet	20 of 62
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Date:	Thursday, February 24, 2011	Sheet	20 of 62																																												



To HDMI-out

To 2D/3D Vision

To 3D Vision

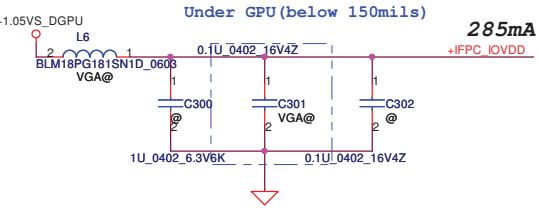
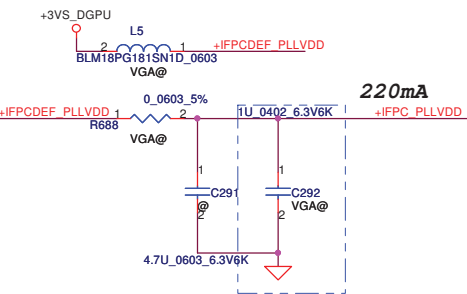
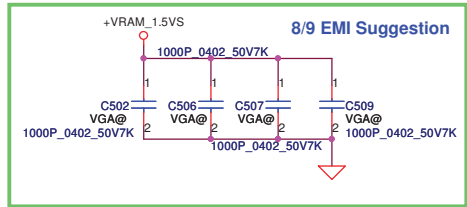
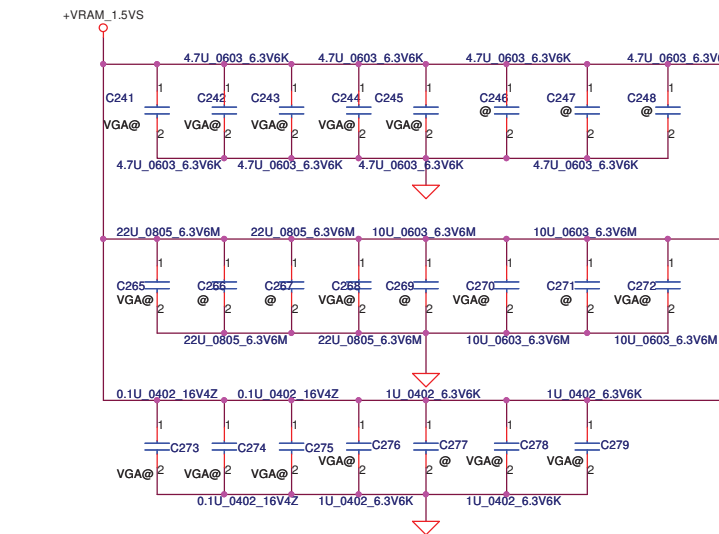
HDMI-OUT

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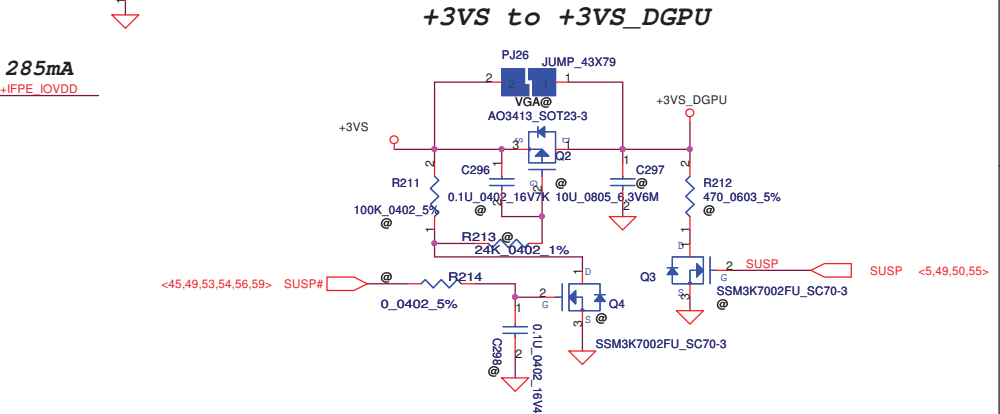
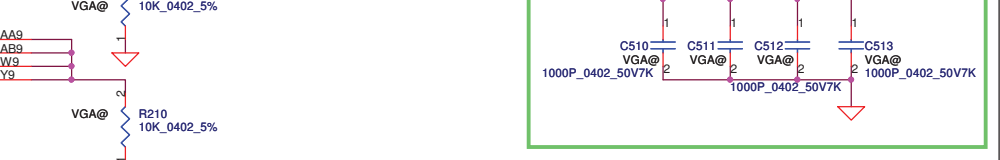
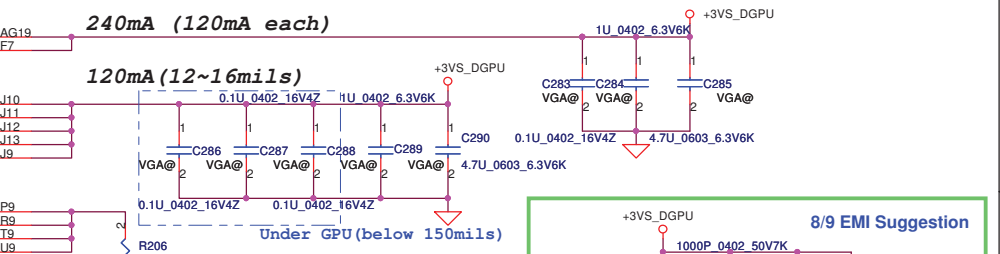
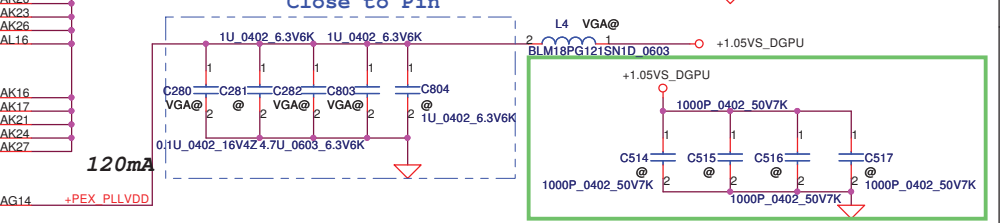
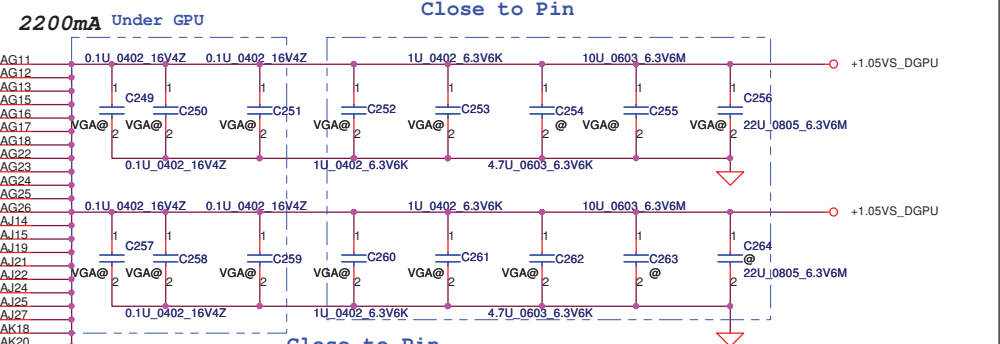




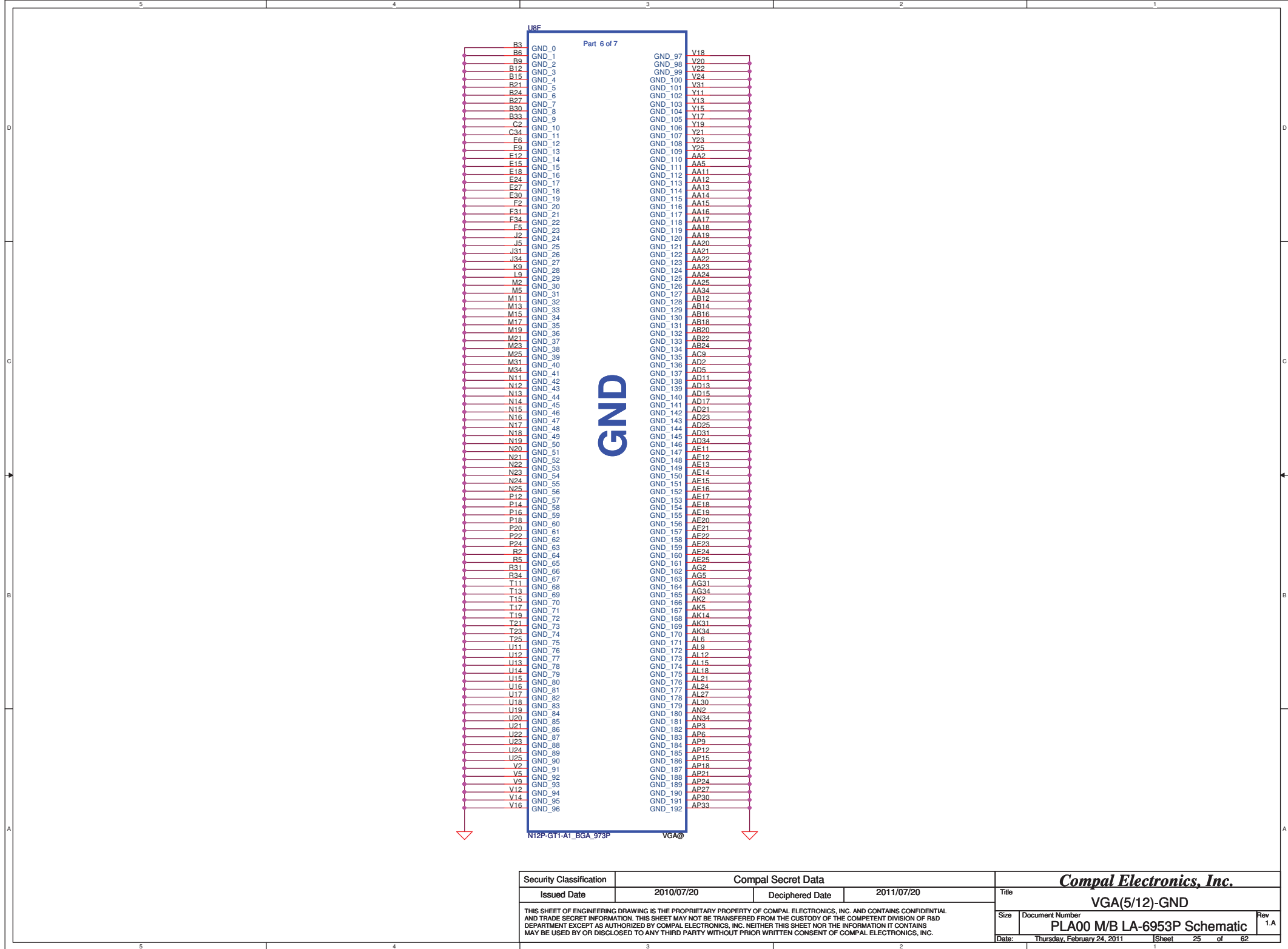
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  - AB27 FBVDDQ\_5
  - AB29 FBVDDQ\_6
  - AC27 FBVDDQ\_7
  - AD27 FBVDDQ\_8
  - AE27 FBVDDQ\_9
  - AJ28 FBVDDQ\_10
  - B18 FBVDDQ\_11
  - E21 FBVDDQ\_12
  - G17 FBVDDQ\_13
  - G18 FBVDDQ\_14
  - G22 FBVDDQ\_15
  - G8 FBVDDQ\_16
  - G9 FBVDDQ\_17
  - H29 FBVDDQ\_18
  - J14 FBVDDQ\_19
  - J15 FBVDDQ\_20
  - J16 FBVDDQ\_21
  - J17 FBVDDQ\_22
  - J20 FBVDDQ\_23
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  - N27 FBVDDQ\_26
  - P27 FBVDDQ\_27
  - R27 FBVDDQ\_28
  - T27 FBVDDQ\_29
  - U27 FBVDDQ\_30
  - V27 FBVDDQ\_31
  - V29 FBVDDQ\_32
  - V34 FBVDDQ\_33
  - W27 FBVDDQ\_34
  - Y27 FBVDDQ\_35
  - Y27 FBVDDQ\_36
  - Y27 FBVDDQ\_37

POWER

- Part 5 of 7
- PEX\_IOVDDQ\_0
- PEX\_IOVDDQ\_1
- PEX\_IOVDDQ\_2
- PEX\_IOVDDQ\_3
- PEX\_IOVDDQ\_4
- PEX\_IOVDDQ\_5
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- PEX\_IOVDDQ\_36
- PEX\_IOVDDQ\_37
- PEX\_SVDD\_3V3
- PEX\_SVDD\_3V3\_NC
- VDD33\_0
- VDD33\_1
- VDD33\_2
- VDD33\_3
- VDD33\_4
- MIOA\_VDDQ\_NC\_0
- MIOA\_VDDQ\_NC\_1
- MIOA\_VDDQ\_NC\_2
- MIOA\_VDDQ\_NC\_3
- MIOB\_VDDQ\_NC\_0
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- MIOB\_VDDQ\_NC\_2
- MIOB\_VDDQ\_NC\_3
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- IFPAB\_RSET
- IFPA\_IOVDD
- IFPB\_IOVDD
- IFPC\_PLLVDD
- IFPC\_RSET
- IFPC\_IOVDD
- IFPD\_PLLVDD
- IFPD\_RSET
- IFPD\_IOVDD
- IFPEF\_PLLVDD
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- VGA@

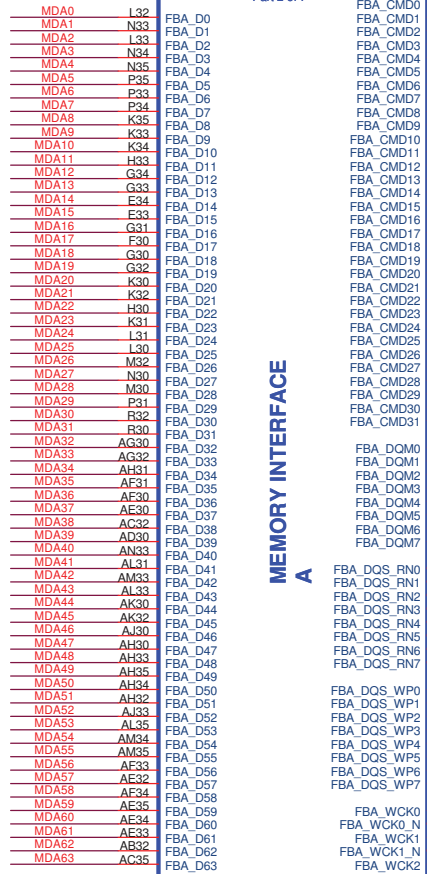


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Size	Document Number	PLA00 M/B LA-6953P Schematic		Rev	1.A
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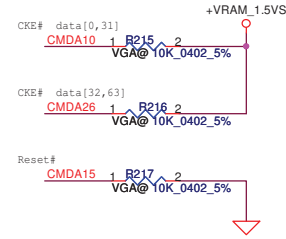
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		Size	Document Number	PLA00 M/B LA-6953P Schematic					Rev	1.A	
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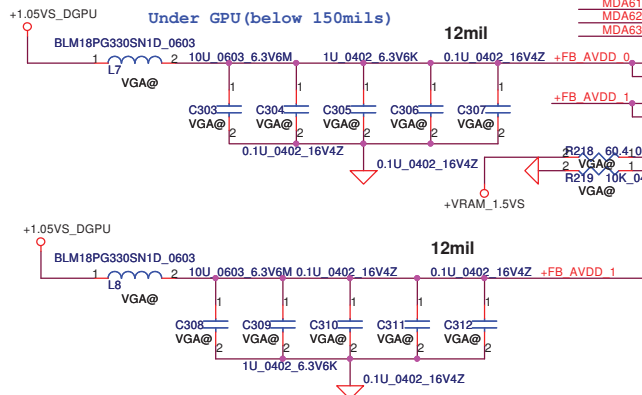
Part 2 of 7

MEMORY INTERFACE  
A



## Mode G- Mapping

Address	DATA Bus
CMD3	A4_BA2
CMD8	ABI#
CMD2	A2_BA0
CMD7	A6_A11
CMD15	RESET#
CMD13	RAS#
CMD4	A5_BA1
CMD6	A7_A8
CMD12	A0_A10
CMD10	CKE#
CMD9	A12_RFU
CMD1	A3_BA3
CMD11	A1_A9
CMD0	CS#
CMD5	WE#
CMD14	CAS#
CMD30	RAS#
CMD20	A3_BA3
CMD16	WE#
CMD25	A12_RFU
CMD28	A7_A8
CMD22	A0_A10
CMD19	A2_BA0
CMD17	A5_BA1
CMD27	A6_A11
CMD29	CAS#
CMD18	A4_BA2
CMD15	RESET#
CMD26	CKE#
CMD23	A1_A9
CMD24	ABI#
CMD21	CS#



<30,31> MDB[0..63]

MDB0 B13  
MDB1 D13  
MDB2 A13  
MDB3 A14  
MDB4 C16  
MDB5 B16  
MDB6 A17  
MDB7 D16  
MDB8 C13  
MDB9 B11  
MDB10 C11  
MDB11 A11  
MDB12 C10  
MDB13 B8  
MDB14 B8  
MDB15 A8  
MDB16 A8  
MDB17 F8  
MDB18 F8  
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MDB54 B35  
MDB55 B34  
MDB56 A29  
MDB57 B28  
MDB58 A28  
MDB59 C26  
MDB60 D25  
MDB61 D25  
MDB62 B25  
MDB63 A25

U8C

Part 3 of 7

MEMORY INTERFACE C

FBC\_CMD0 E18  
FBC\_CMD1 E19  
FBC\_CMD2 G17  
FBC\_CMD3 E19  
FBC\_CMD4 C19  
FBC\_CMD5 C19  
FBC\_CMD6 B17  
FBC\_CMD7 E20  
FBC\_CMD8 B19  
FBC\_CMD9 D20  
FBC\_CMD10 A19  
FBC\_CMD11 D19  
FBC\_CMD12 C20  
FBC\_CMD13 F20  
FBC\_CMD14 B20  
FBC\_CMD15 G21  
FBC\_CMD16 F22  
FBC\_CMD17 F24  
FBC\_CMD18 E23  
FBC\_CMD19 C25  
FBC\_CMD20 C23  
FBC\_CMD21 E22  
FBC\_CMD22 D21  
FBC\_CMD23 A23  
FBC\_CMD24 A23  
FBC\_CMD25 D22  
FBC\_CMD26 B23  
FBC\_CMD27 C22  
FBC\_CMD28 B22  
FBC\_CMD29 A22  
FBC\_CMD30 A20  
FBC\_CMD31 G20

FBC\_DOM0 A16  
FBC\_DOM1 D10  
FBC\_DOM2 D10  
FBC\_DOM3 D15  
FBC\_DOM4 D27  
FBC\_DOM5 D34  
FBC\_DOM6 A34  
FBC\_DOM7 D28

FBC\_DQS\_RN0 B14  
FBC\_DQS\_RN1 B10  
FBC\_DQS\_RN2 D9  
FBC\_DQS\_RN3 E14  
FBC\_DQS\_RN4 F26  
FBC\_DQS\_RN5 D31  
FBC\_DQS\_RN6 A31  
FBC\_DQS\_RN7 A26

FBC\_DQS\_WP0 C14  
FBC\_DQS\_WP1 A10  
FBC\_DQS\_WP2 E10  
FBC\_DQS\_WP3 D14  
FBC\_DQS\_WP4 F26  
FBC\_DQS\_WP5 D32  
FBC\_DQS\_WP6 A32  
FBC\_DQS\_WP7 B26

FBC\_WCK0 G14  
FBC\_WCK0\_N G15  
FBC\_WCK1 G11  
FBC\_WCK1\_N G12  
FBC\_WCK2 G27  
FBC\_WCK2\_N G28  
FBC\_WCK3 G24  
FBC\_WCK3\_N G25

FBC\_CLK0 E17  
FBC\_CLK0\_N D17  
FBC\_CLK1 D23  
FBC\_CLK1\_N E23

CMDB0 E18  
CMDB1 E19  
CMDB2 G17  
CMDB3 E19  
CMDB4 C19  
CMDB5 C19  
CMDB6 B17  
CMDB7 E20  
CMDB8 B19  
CMDB9 D20  
CMDB10 A19  
CMDB11 D19  
CMDB12 C20  
CMDB13 F20  
CMDB14 B20  
CMDB15 G21  
CMDB16 F22  
CMDB17 F24  
CMDB18 E23  
CMDB19 C25  
CMDB20 C23  
CMDB21 E22  
CMDB22 D21  
CMDB23 A23  
CMDB24 A23  
CMDB25 D22  
CMDB26 B23  
CMDB27 C22  
CMDB28 B22  
CMDB29 A22  
CMDB30 A20  
CMDB31 G20

DOMB0 A16  
DOMB1 D10  
DOMB2 D10  
DOMB3 D15  
DOMB4 D27  
DOMB5 D34  
DOMB6 A34  
DOMB7 D28

DQS0 B14  
DQS1 B10  
DQS2 D9  
DQS3 E14  
DQS4 F26  
DQS5 D31  
DQS6 A31  
DQS7 A26

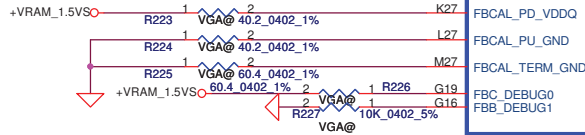
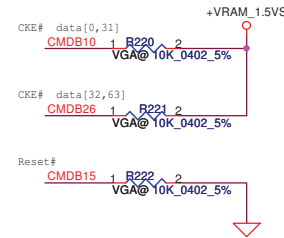
DQS8 C14  
DQS9 A10  
DQS10 E10  
DQS11 D14  
DQS12 F26  
DQS13 D32  
DQS14 A32  
DQS15 B26

FBB\_WCK0 G14  
FBB\_WCK01# G15  
FBB\_WCK23 G11  
FBB\_WCK23# G12  
FBB\_WCK45 G27  
FBB\_WCK45# G28  
FBB\_WCK67 G24  
FBB\_WCK67# G25

CLKB0 E17  
CLKB0# D17  
CLKB1 D23  
CLKB1# E23

DQMB[7..0] <30,31>

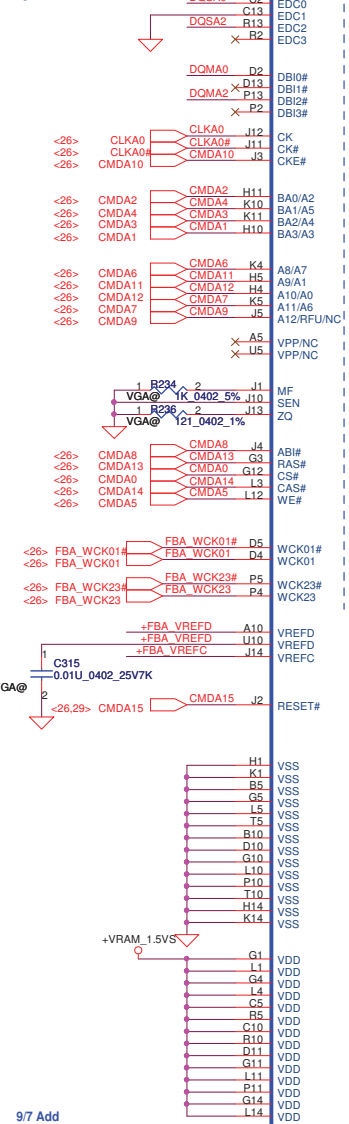
DQSB[7..0] <30,31>



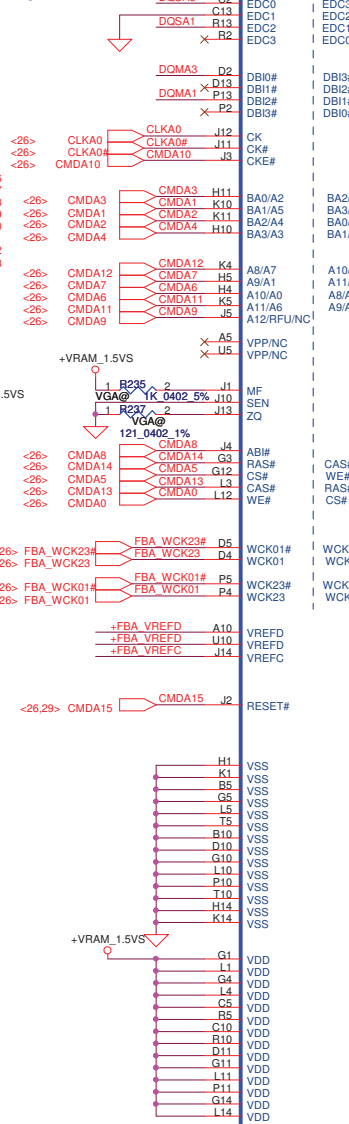
## Mode G- Mapping

DATA Bus		
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

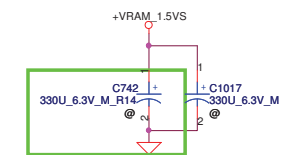
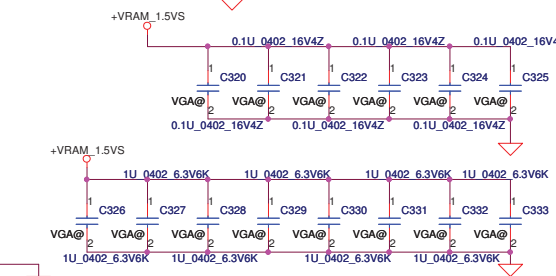
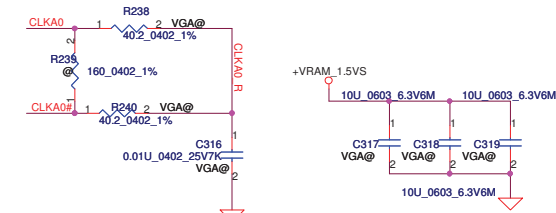
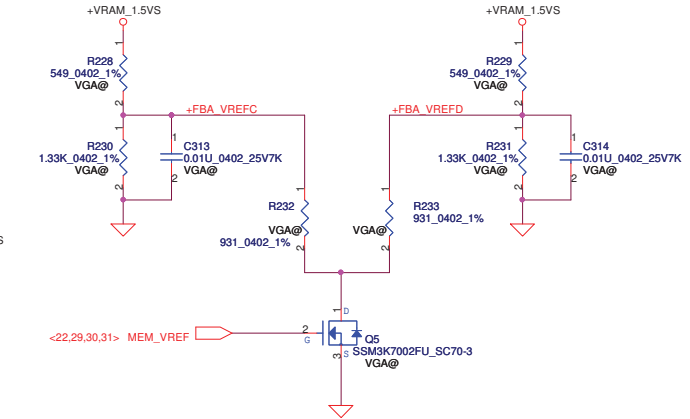
# MF=0 Byte 0 and 2



# MF=1 Byte 1 and 3



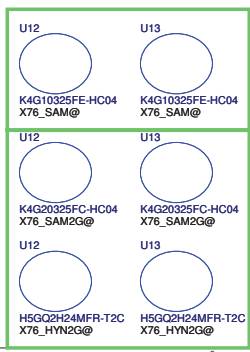
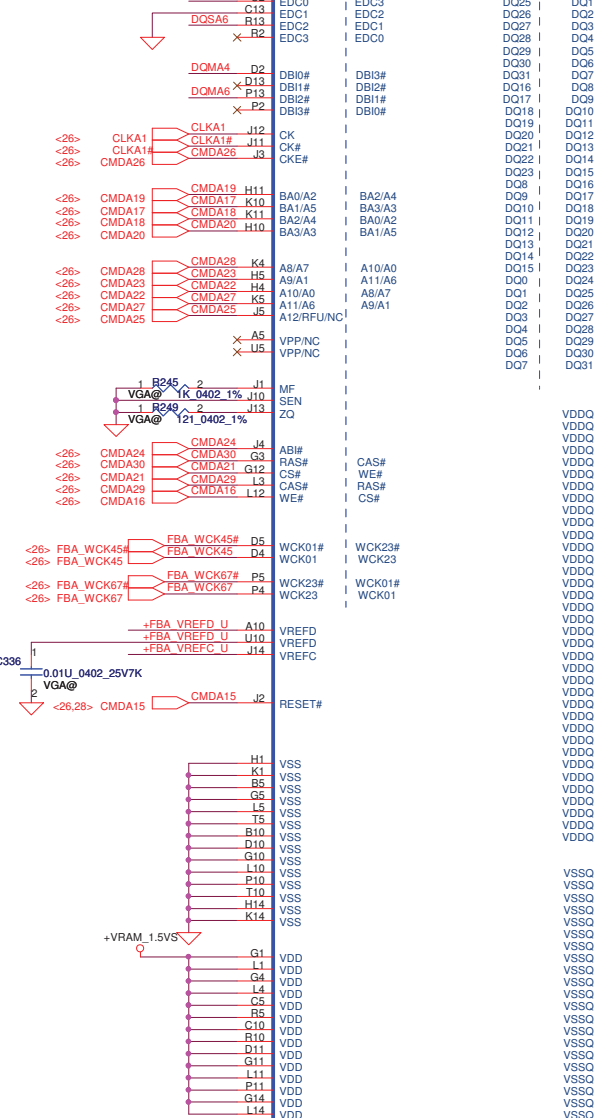
MDA[0..63] <26,29>  
DOMA[7..0] <26,29>  
DQSA[7..0] <26,29>



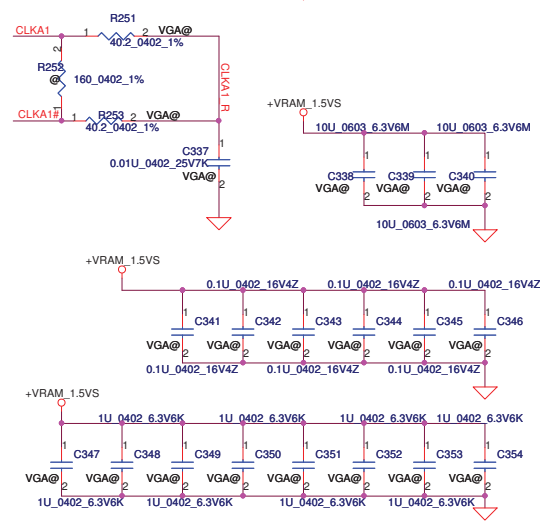
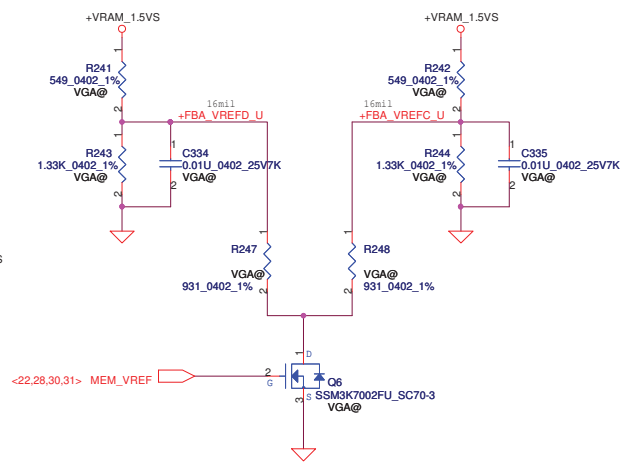
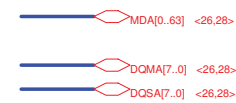
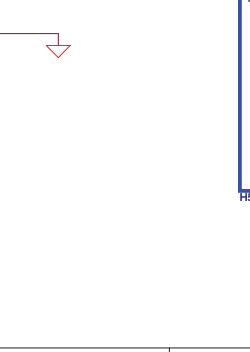
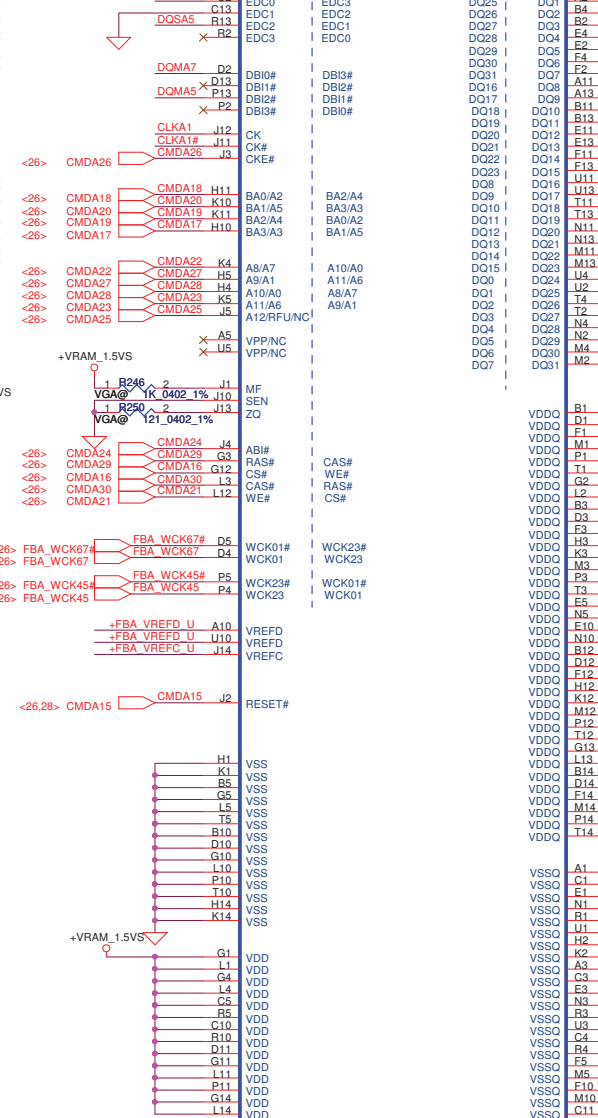
10/23 Change symbol of C742 from SGA20331E10 to SF000002M00  
11/2 Change PN of C742 from SF000002M00 to SF000001G00

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	VRAM_GDDR5 / Channel A	
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				Date: Thursday, February 24, 2011	Sheet 28 of 62

# MF=0 Byte 0 and 2



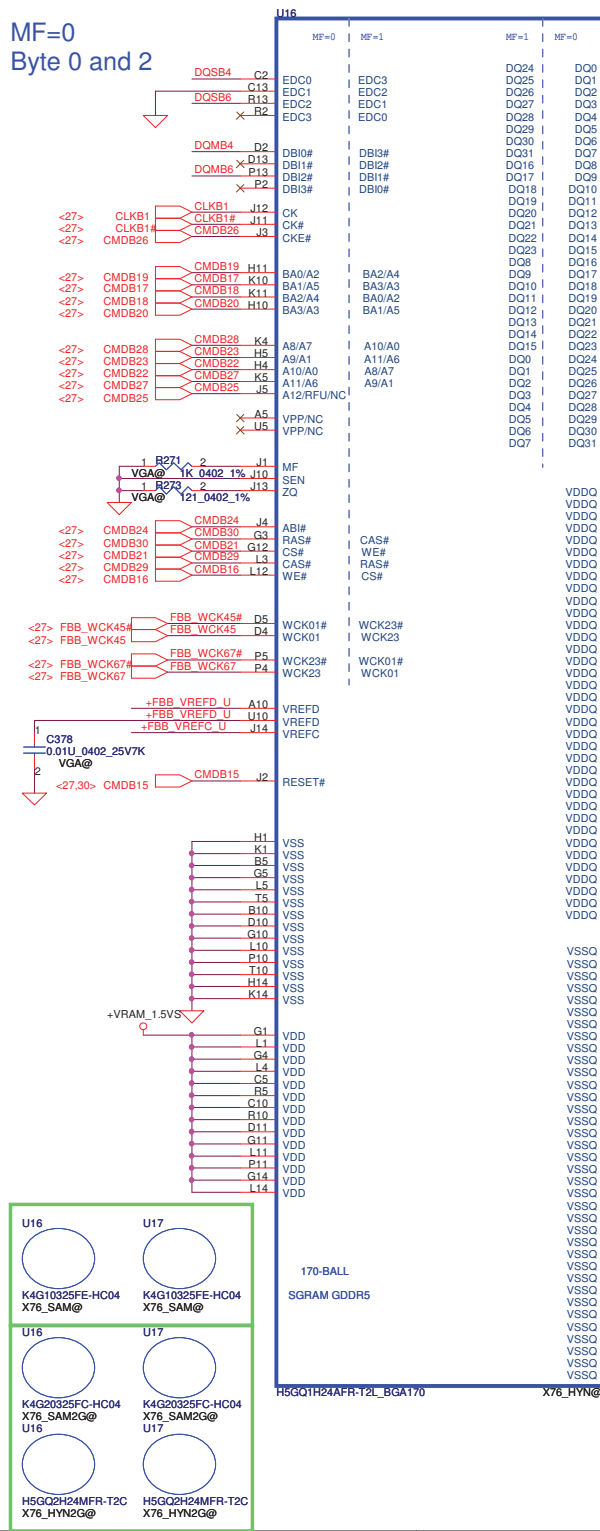
# MF=1 Byte 1 and 3



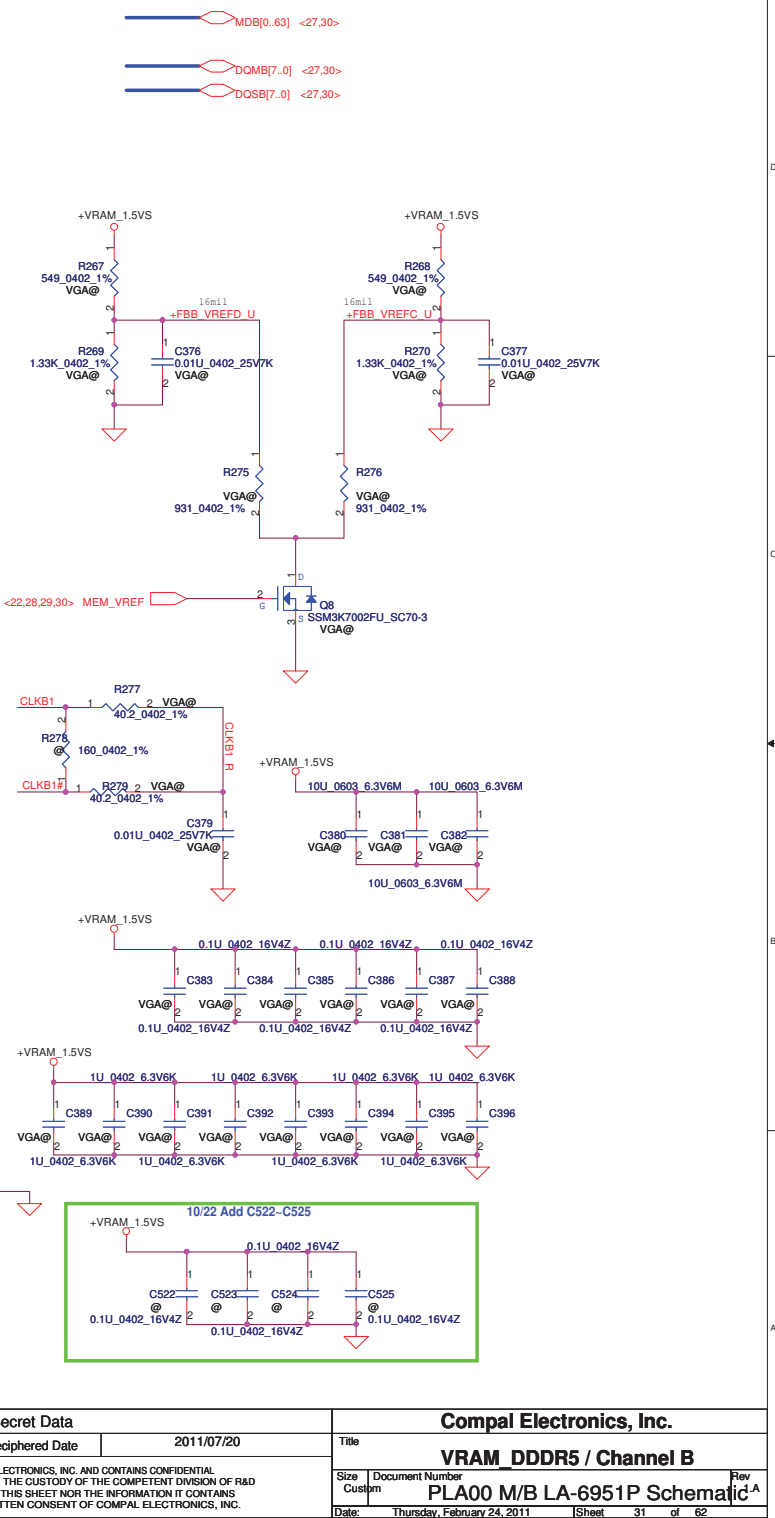
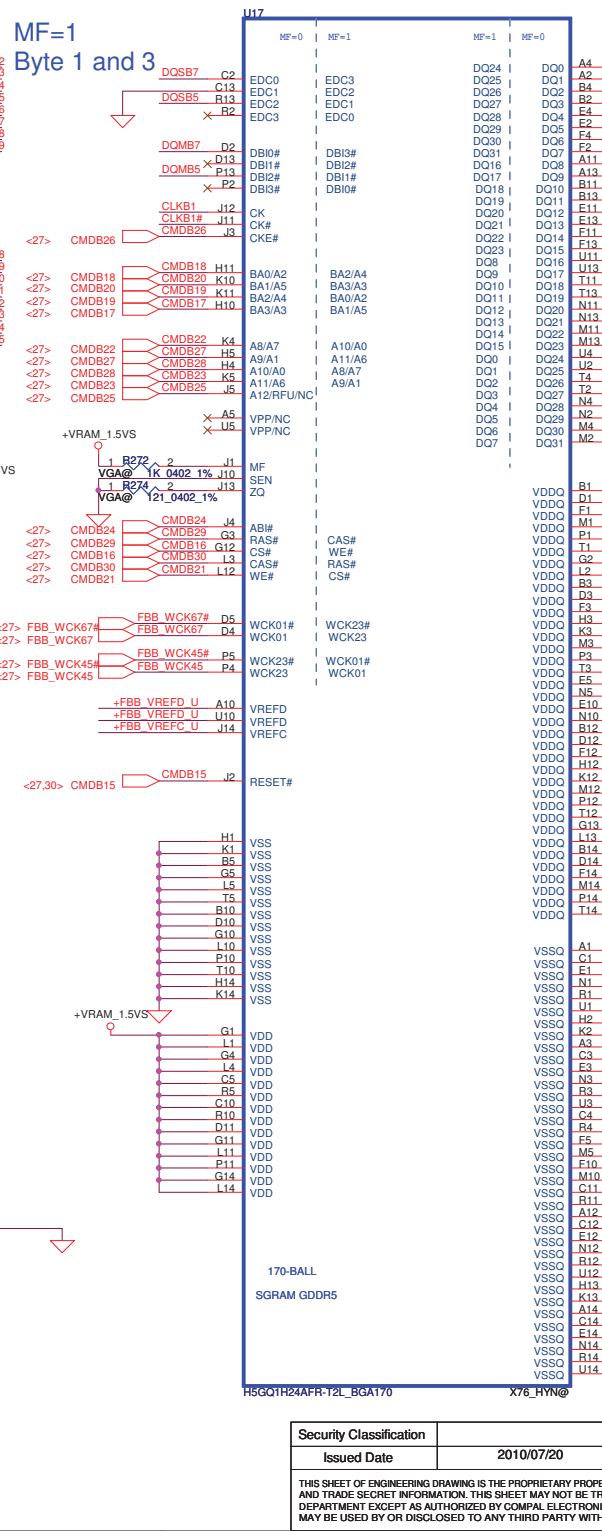
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	VRAM DDR5 / Channel A
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				Custm	PLA00 M/B LA-6951P Schematic
				Date	Thursday, February 24, 2011
				Sheet	29 of 62



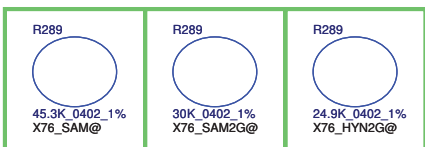
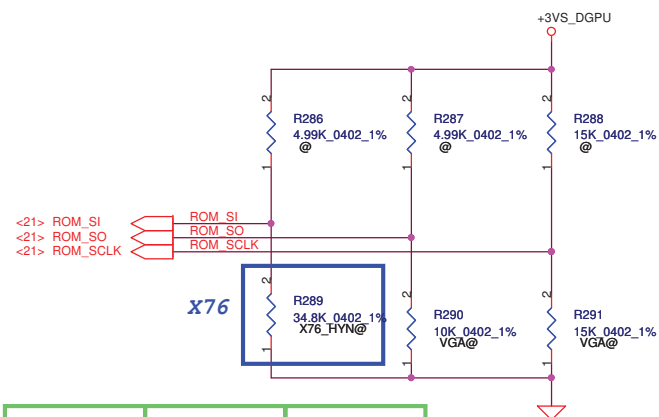
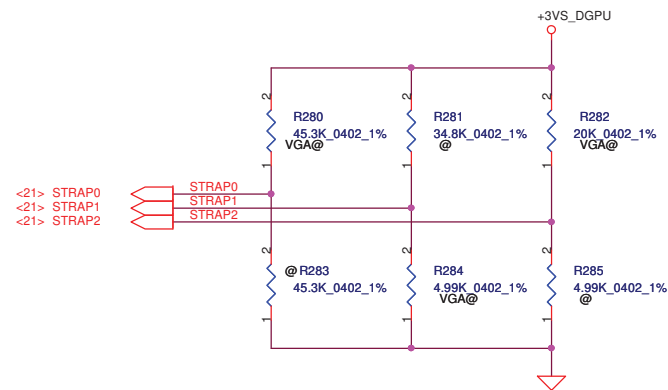
MF=0  
Byte 0 and 2



MF=1  
Byte 1 and 3



Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	VRAM_DDR5 / Channel B	
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				Custom	PLA00 M/B LA-6951P Schematic
				Date:	Thursday, February 24, 2011
				Sheet	31 of 62



Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

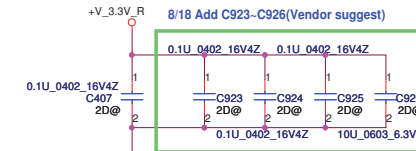
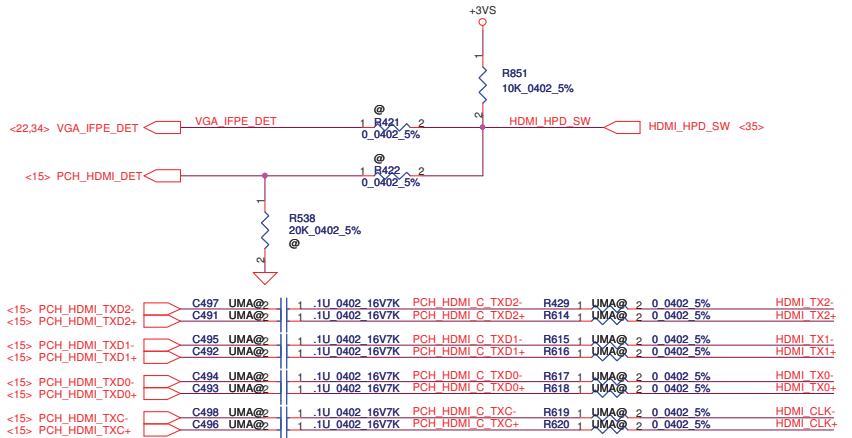
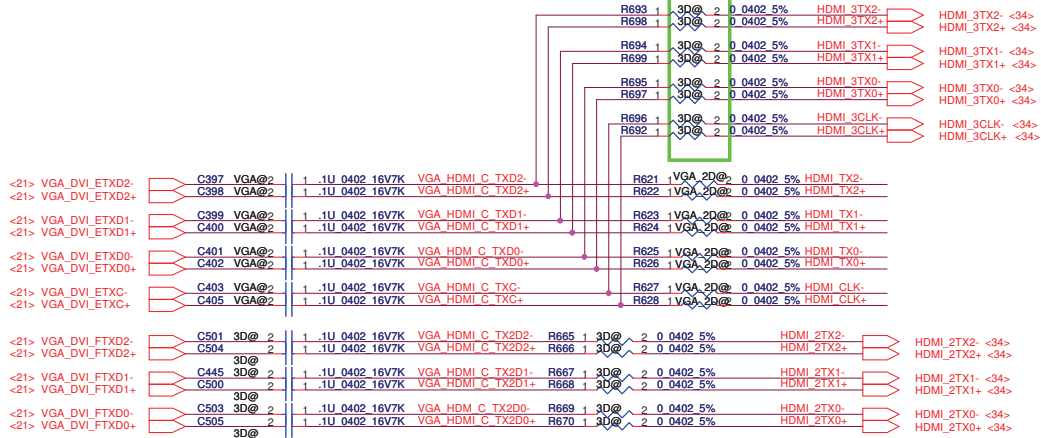
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

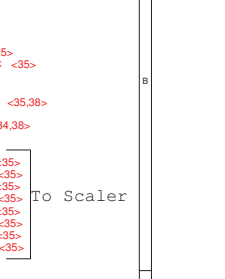
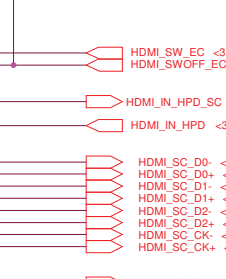
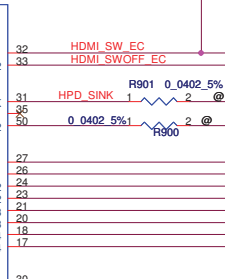
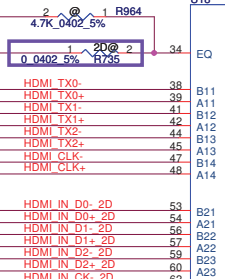
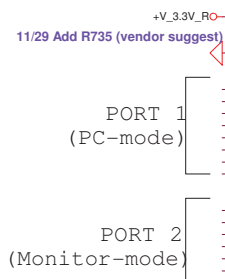
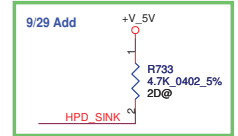
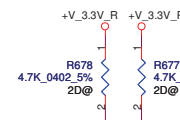
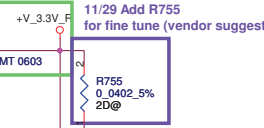
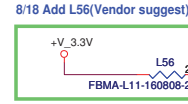
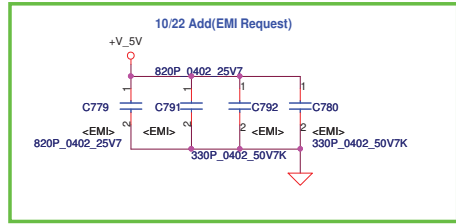
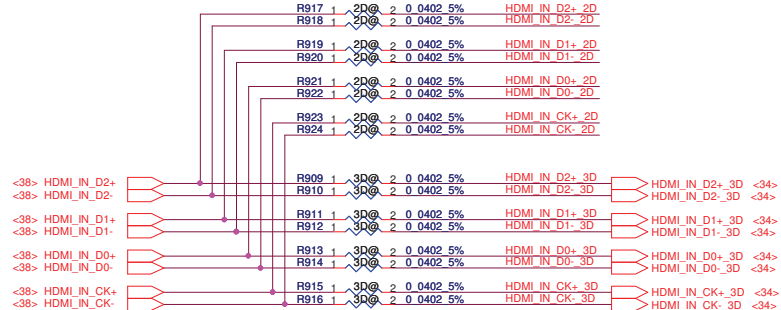
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title
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Size Custom		Document Number		Rev 1.A
Date: Thursday, February 24, 2011		Sheet 32 of 62		

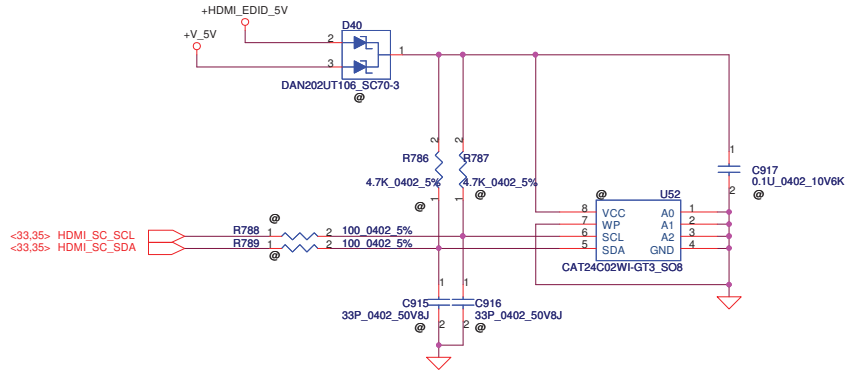
0804 Vendor suggest close to Cap.



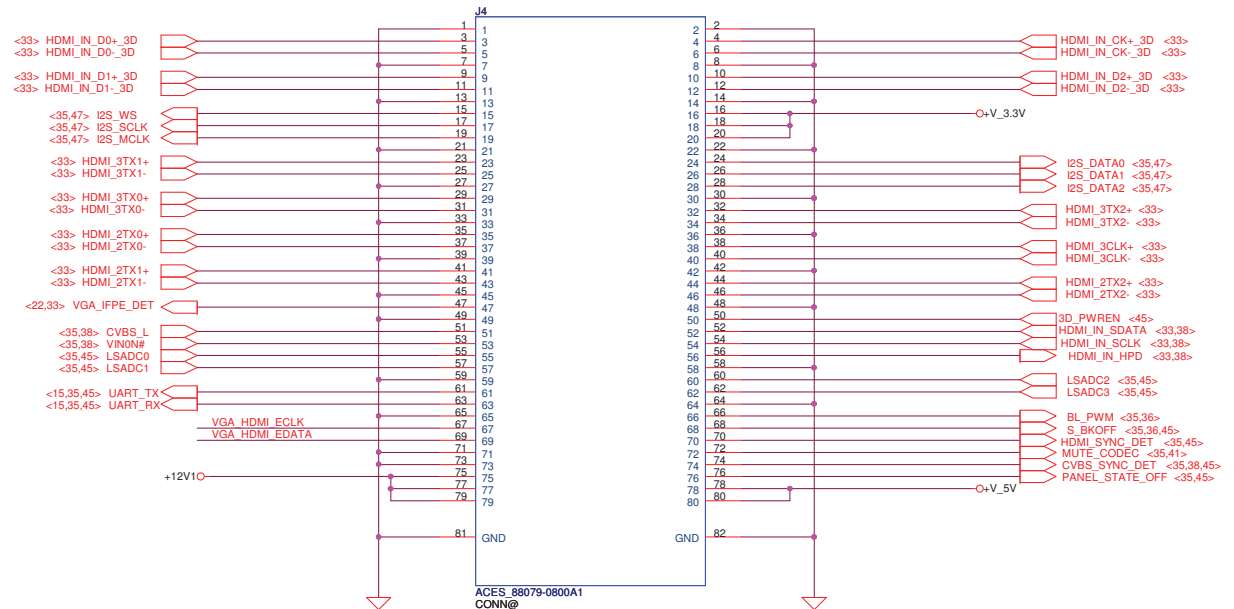
S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1, SDA1
H	L	PORT2/SCL2, SDA2
L	H	All disconnected



# 0810 Vendor suggest to reserve for EDID debug



# 12/11 3D Scaler Pin define update



12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

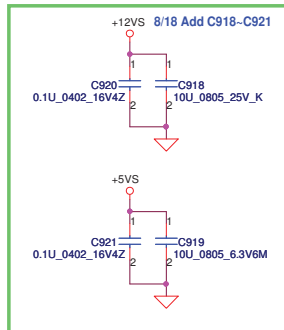


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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	Document Number	PLA00 M/B LA-6951P Schematic		Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	34	of	62



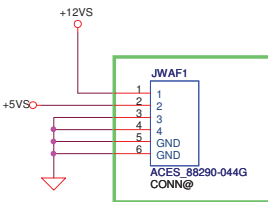


## HDD POWER Conn

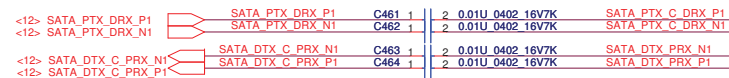


Layout Note: Place C918/C919/C920/C921 close to JWAFER1

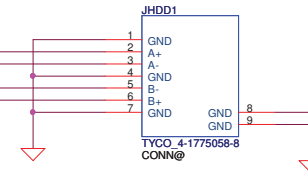
## HDD



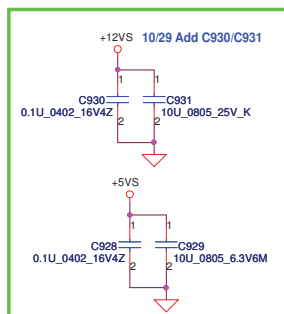
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



## SATA HDD Conn.

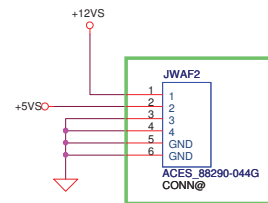


## ODD POWER Conn

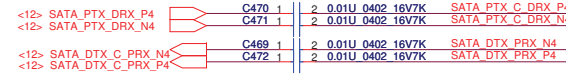


10/28 Add C928/C929

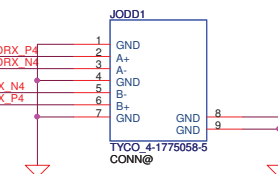
Layout Note: Place C928/C929 close to JWAFER2



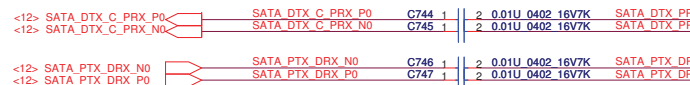
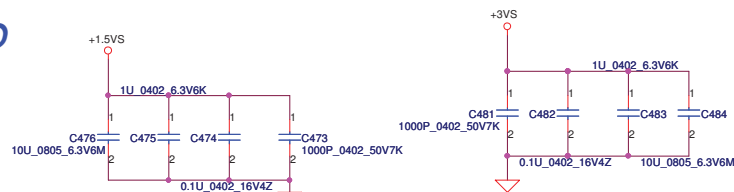
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



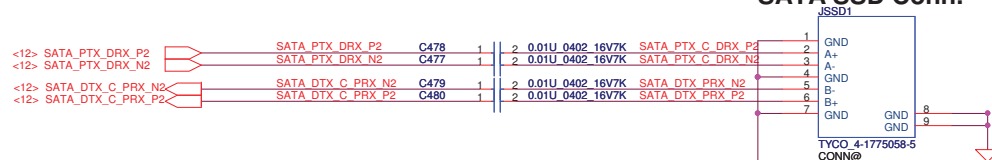
## SATA ODD Conn.



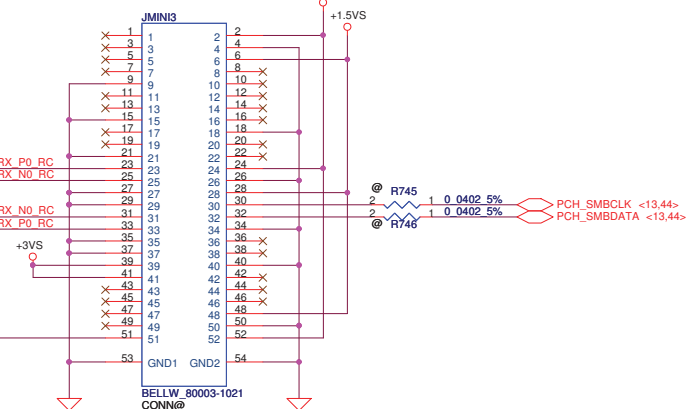
## SSD



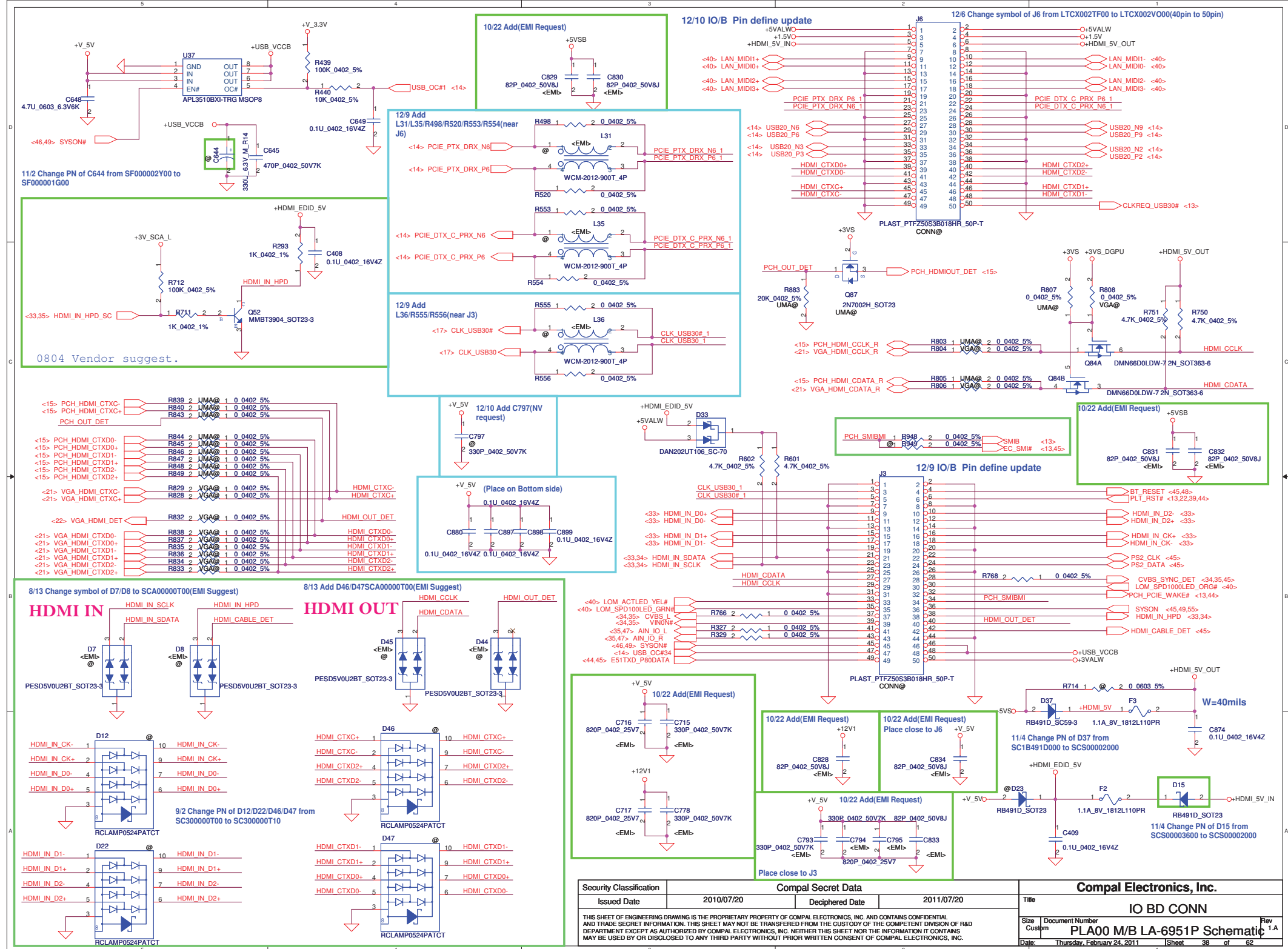
## SATA SSD Conn.

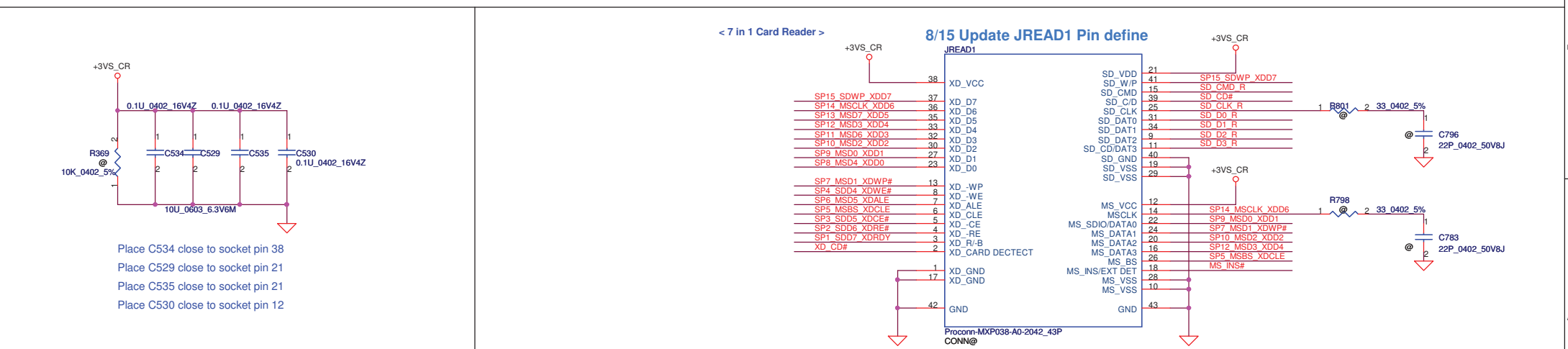
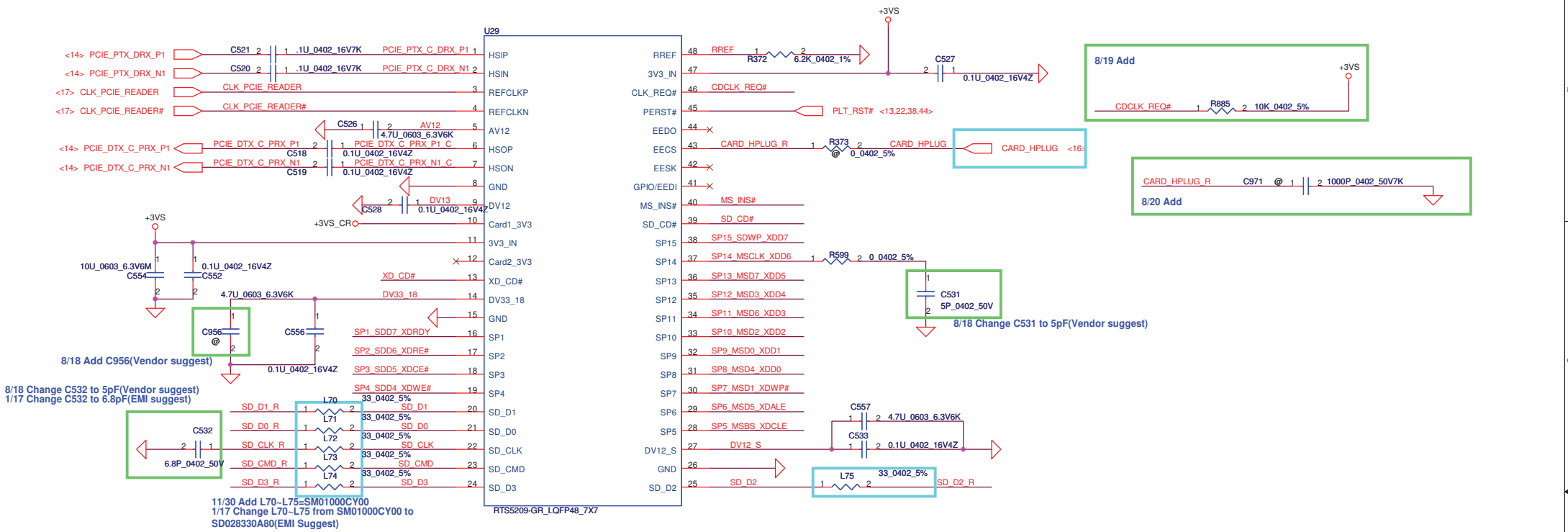


## MINI SSD Conn.



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Size B	Document Number	PLA00 M/B LA-6951P Schematic		Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	37	of	62





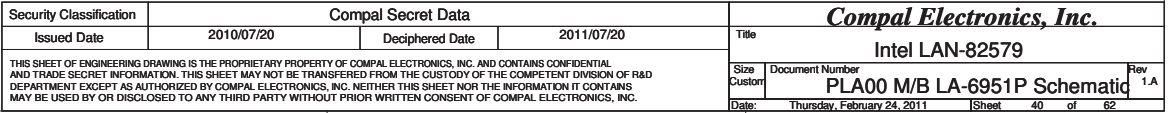
Security Classification			Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2011/07/20		PCIE-Card Reader-RTS5209	
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					Date:	Thursday, February 24, 2011
					Sheet	39 of 62

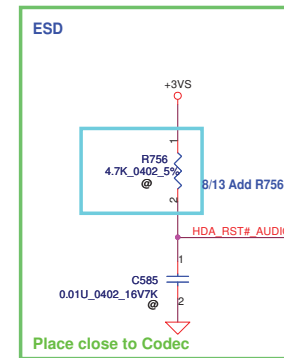
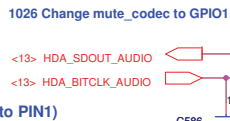
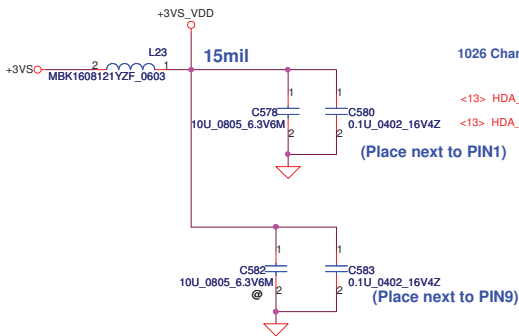
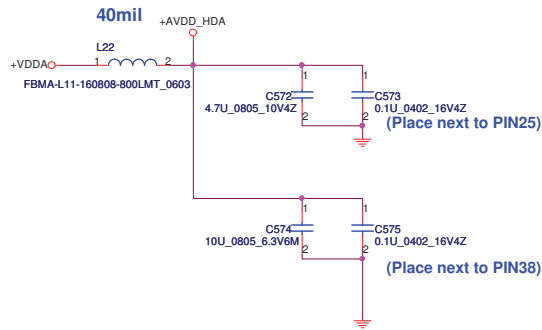
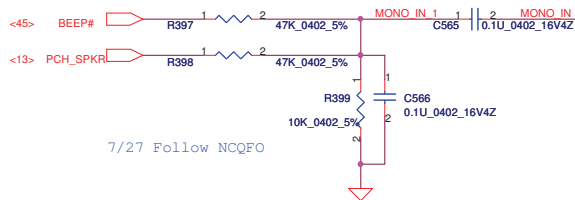
**Compal Electronics, Inc.**

**PCIE-Card Reader-RTS5209**

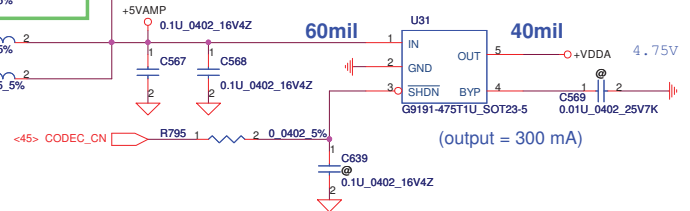
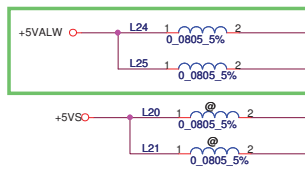
**PLA00 M/B LA-6953P Schematic**

Rev 1.A

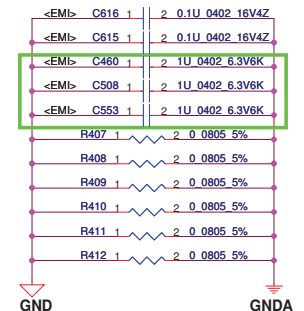
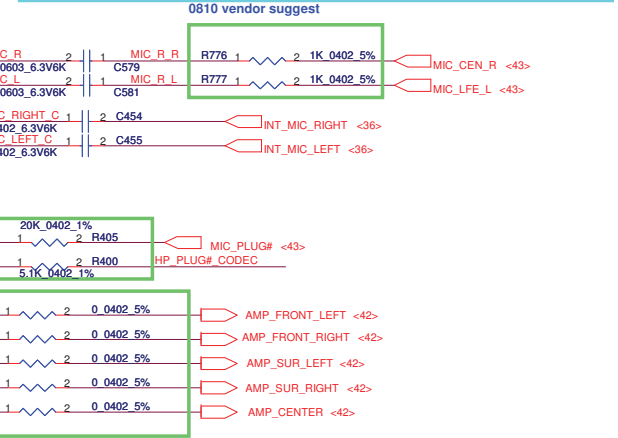
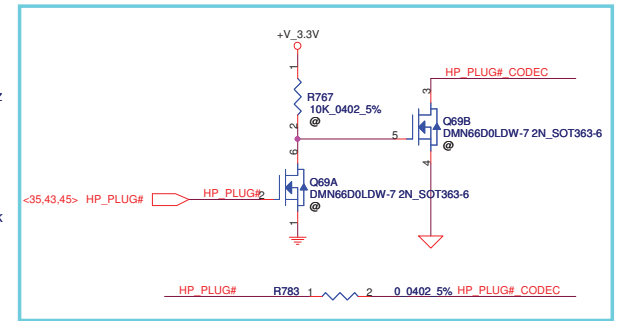
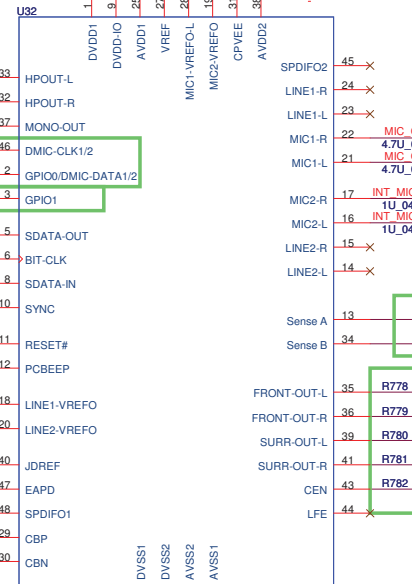
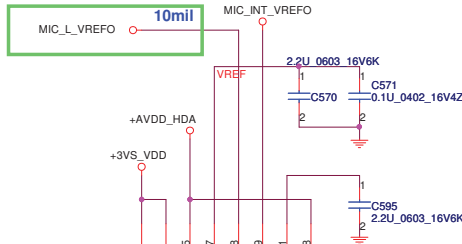




#### 0105 Add L24/L25



#### 1026 DEL MIC\_R\_VREF0



Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

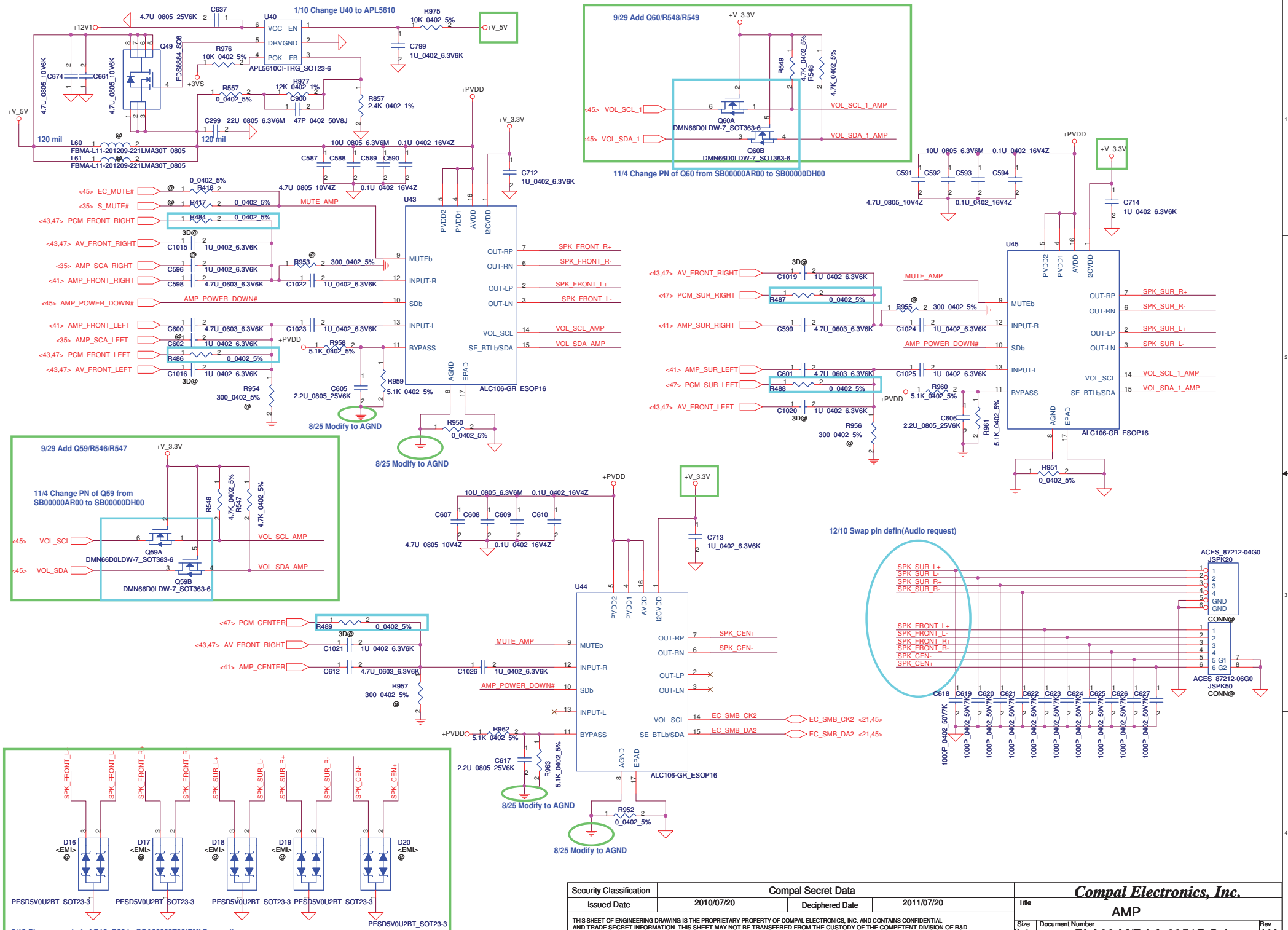
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Date: Thursday, February 24, 2011				Sheet	62

Compal Electronics, Inc.

HD Audio Codec ALC663

PLA00 M/B LA-6951P Schematic

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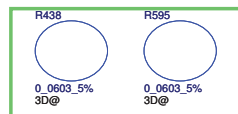
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Issued Date		2010/07/20		Deciphered Date		2011/07/20		Title			
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						Size		Document Number		Rev	
						Custom		PLA00 M/B LA-6951P Schematic		A	
						Date		Thursday, February 24, 2011		Sheet 42 of 62	

1026 Add Diode for MIC\_L\_VREF0  
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00

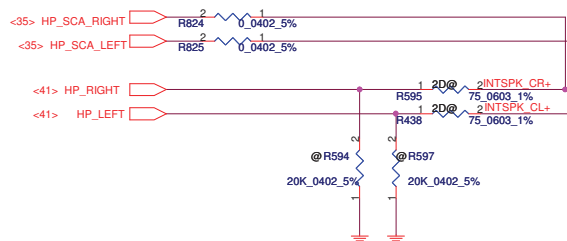
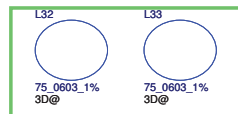
## EXT MIC IN

8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)

2/18 Add



2/24 Add



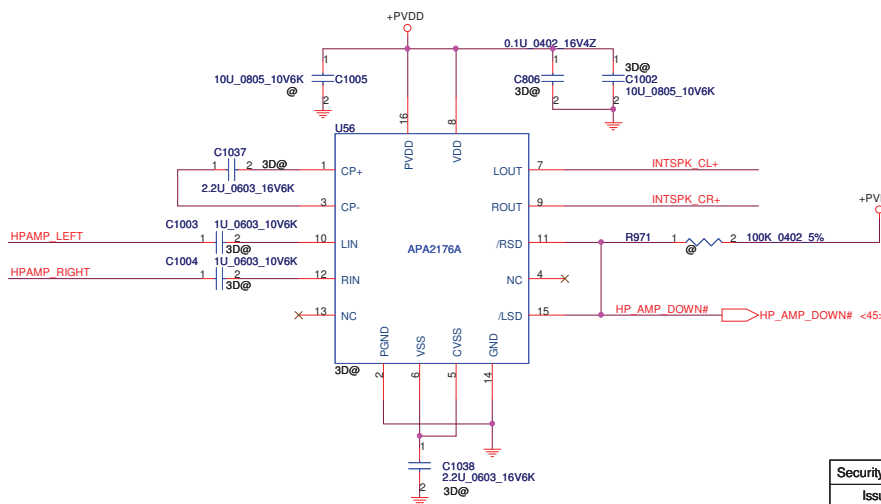
8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

## HP OUT

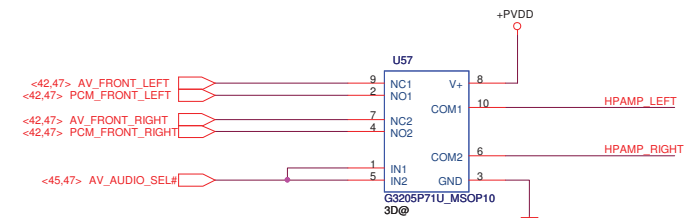
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)

10/22 Change U56 from SA00001ZW00 to SA00004IS00



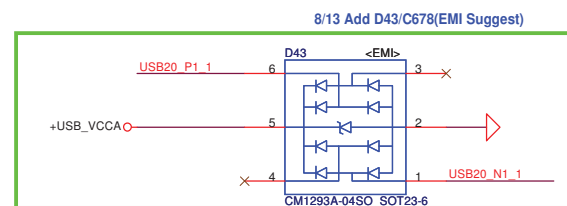
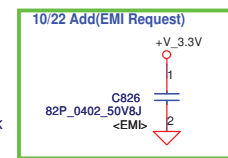
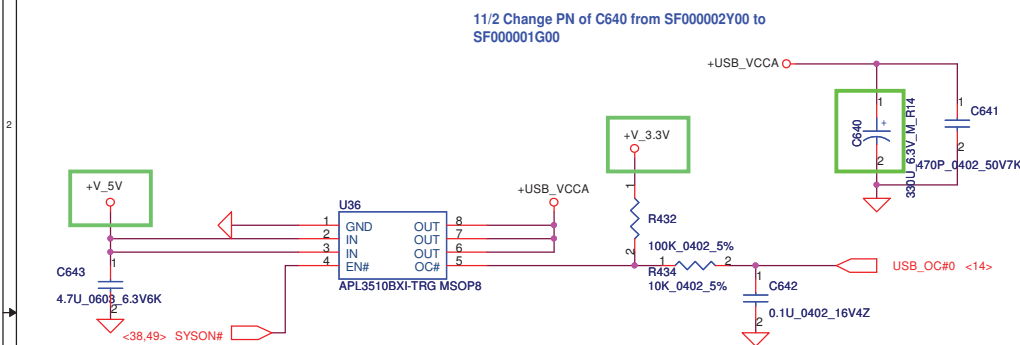
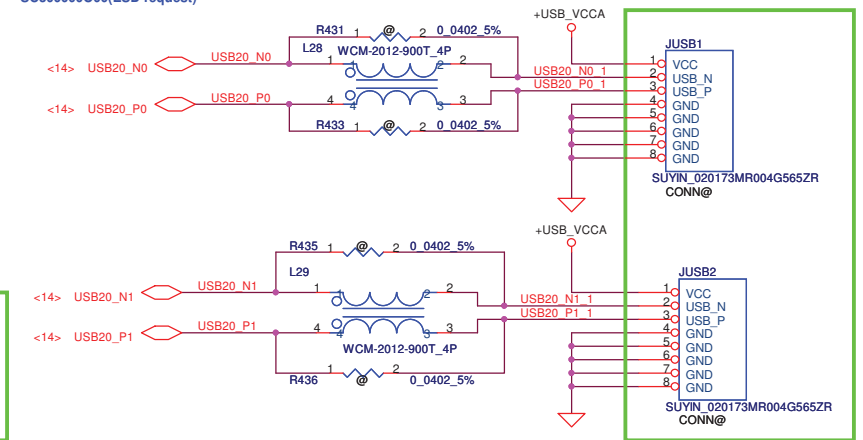
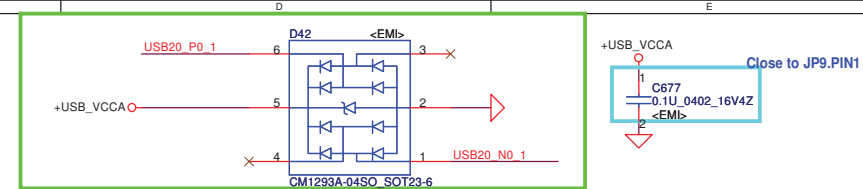
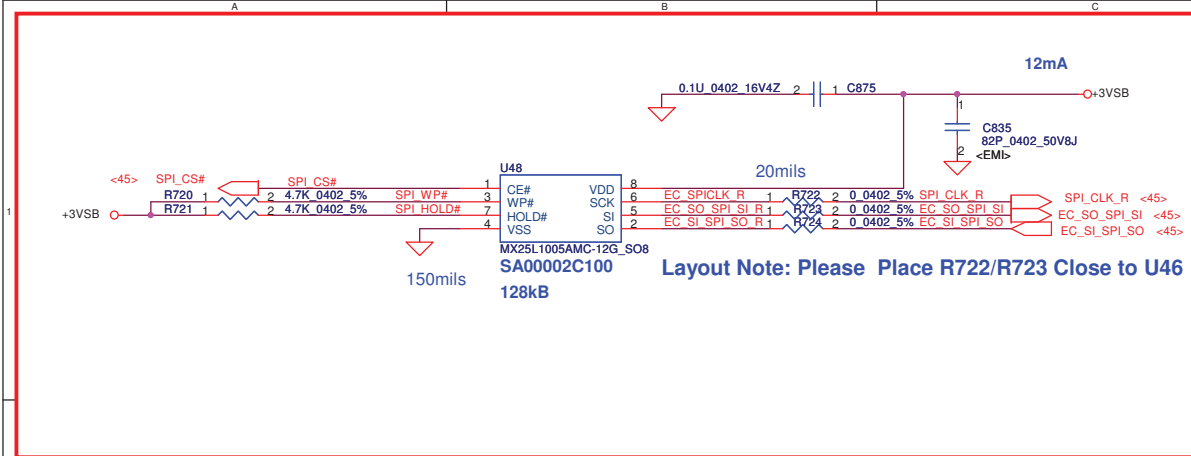
12/09 Add U57



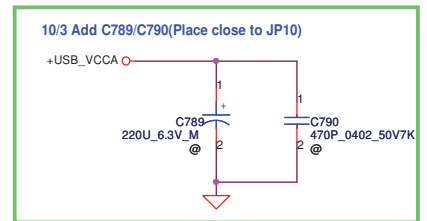
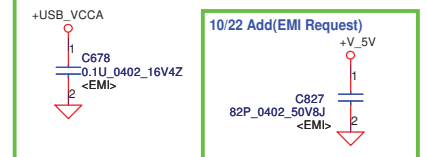
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	Document Number	Customer	Rev	PLA00 M/B LA-6951P Schematic	
Date:	Thursday, February 24, 2011	Sheet	43 of 62	1.A	





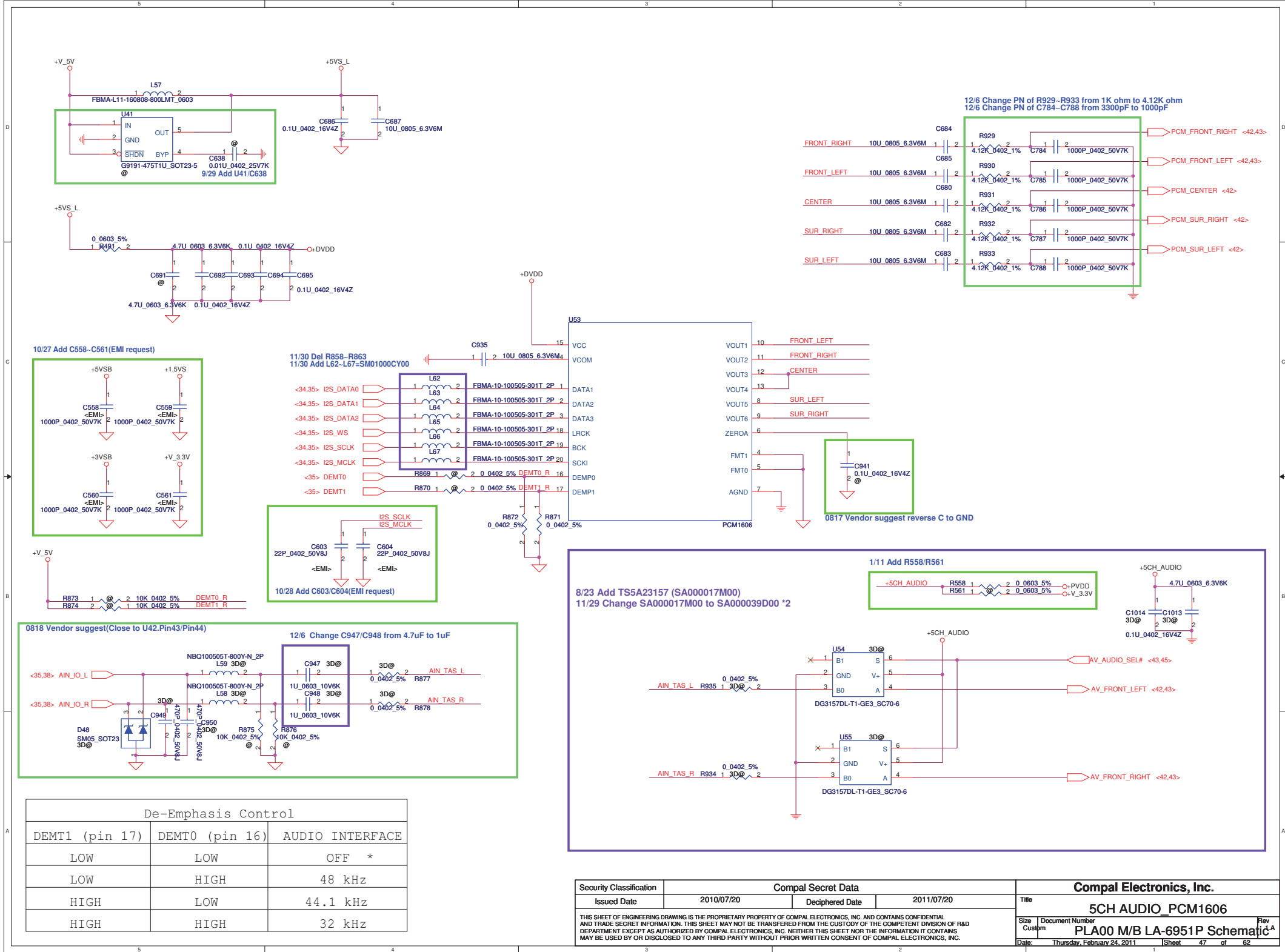


10/25 Change symbol and footprint of D43 from SC300000100 to SC300000000(ESD request)



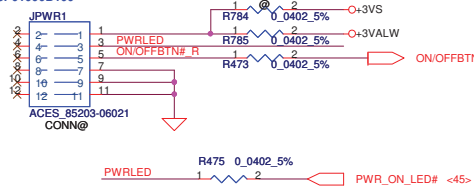
USB Conn. (SIDE)

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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	46	of	62

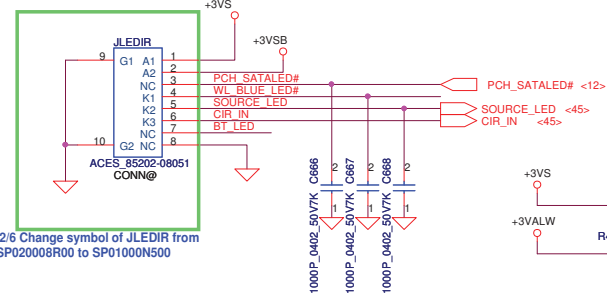


## Power switch board

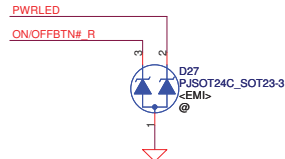
12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100



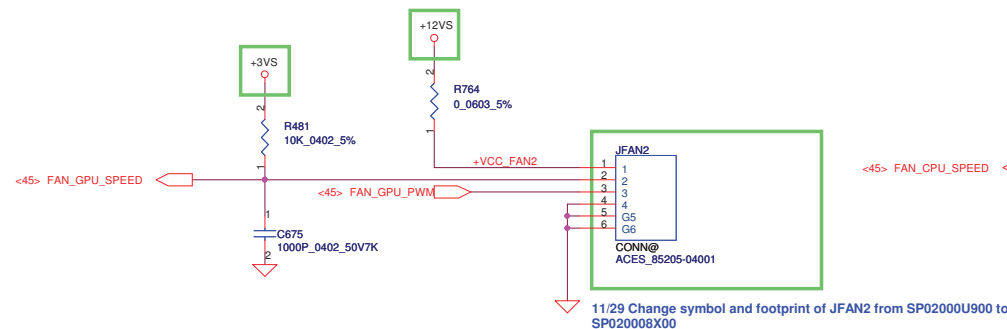
## LED board conn.



8/13 Change symbol of D27 to SCA0000E00(EMI Suggest)

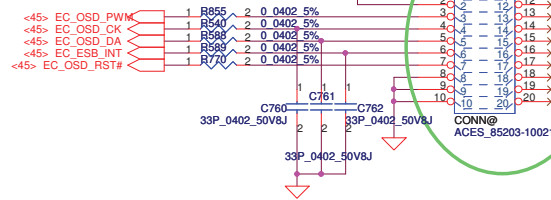


## Fan Control circuit

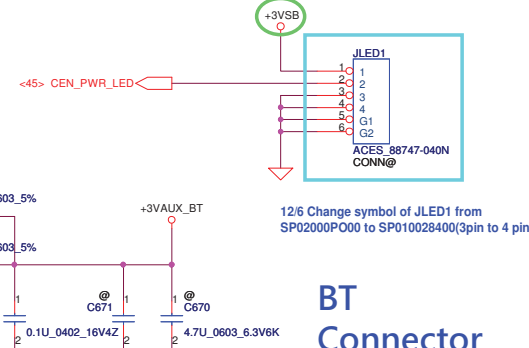


## SENSOR BOTTOM

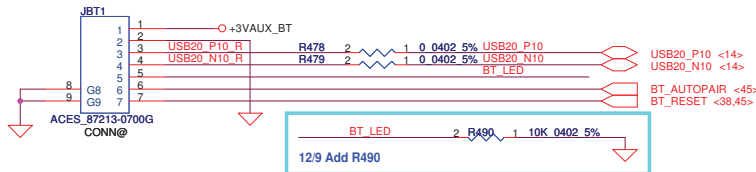
Follow NCQD0



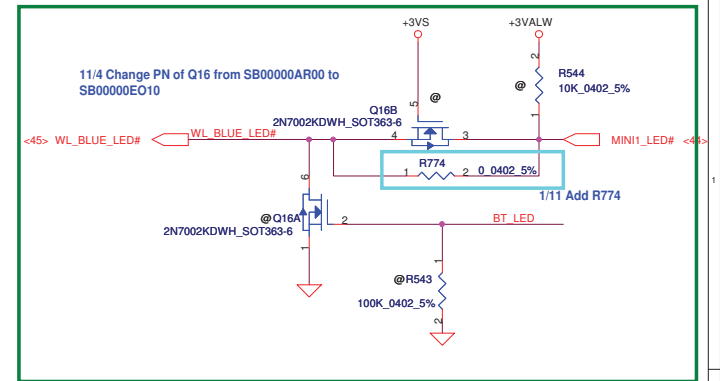
## DECO LED board conn.



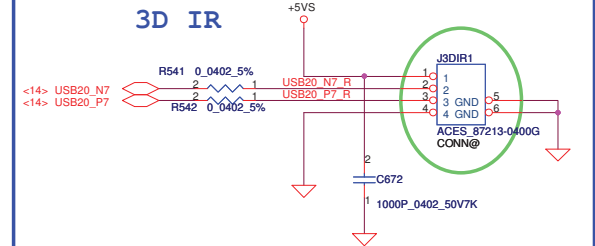
10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000



## BT Connector



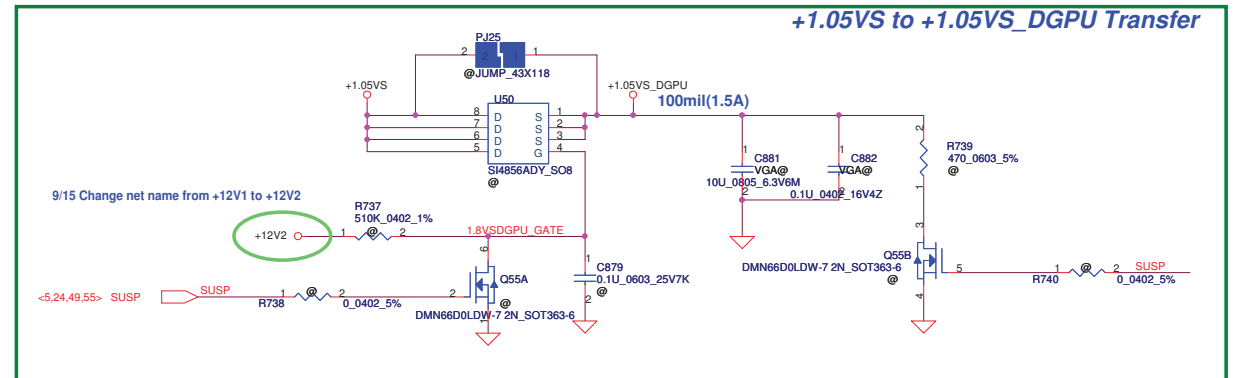
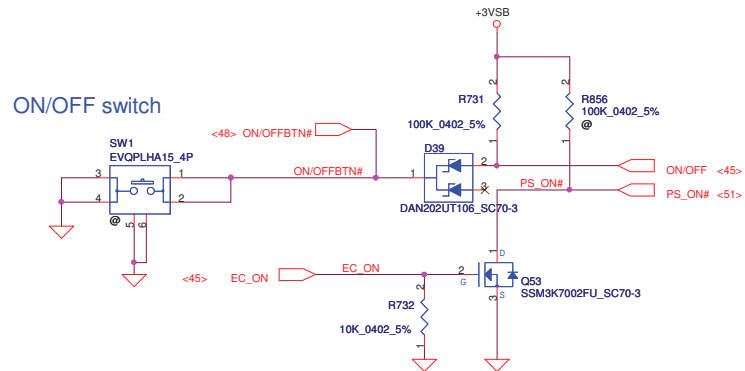
## 3D IR



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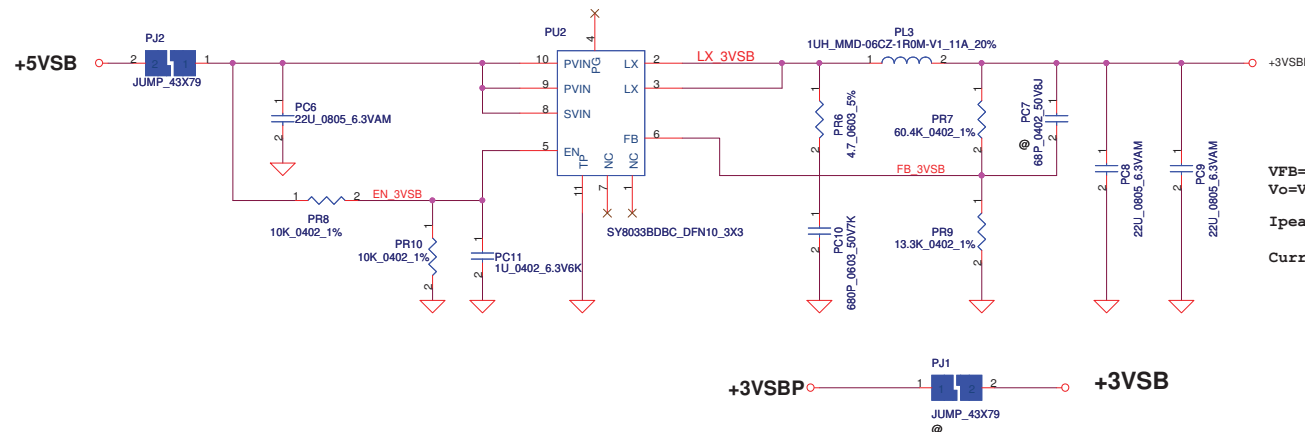
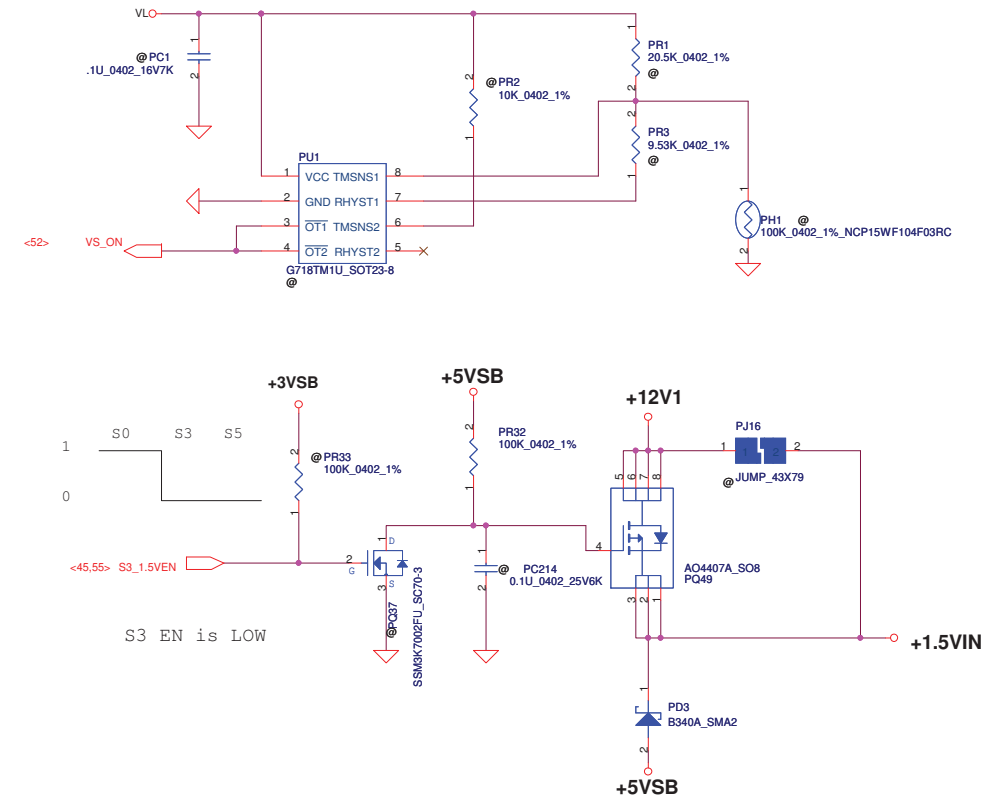
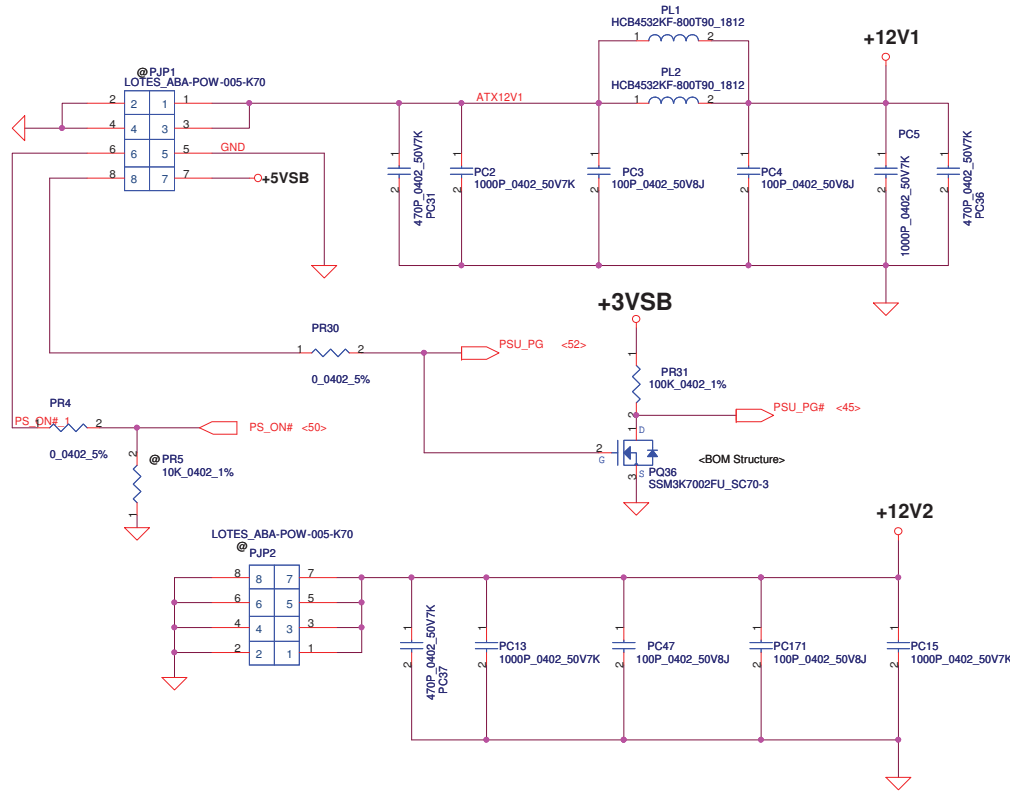
## Power Button



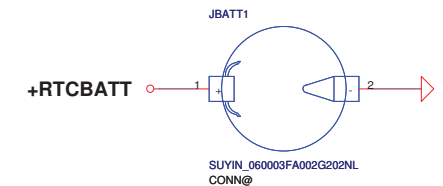
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	Power OK/PBN
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				PLA00 M/B LA-6951P Schematic	
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PH1 under CPU botten side :

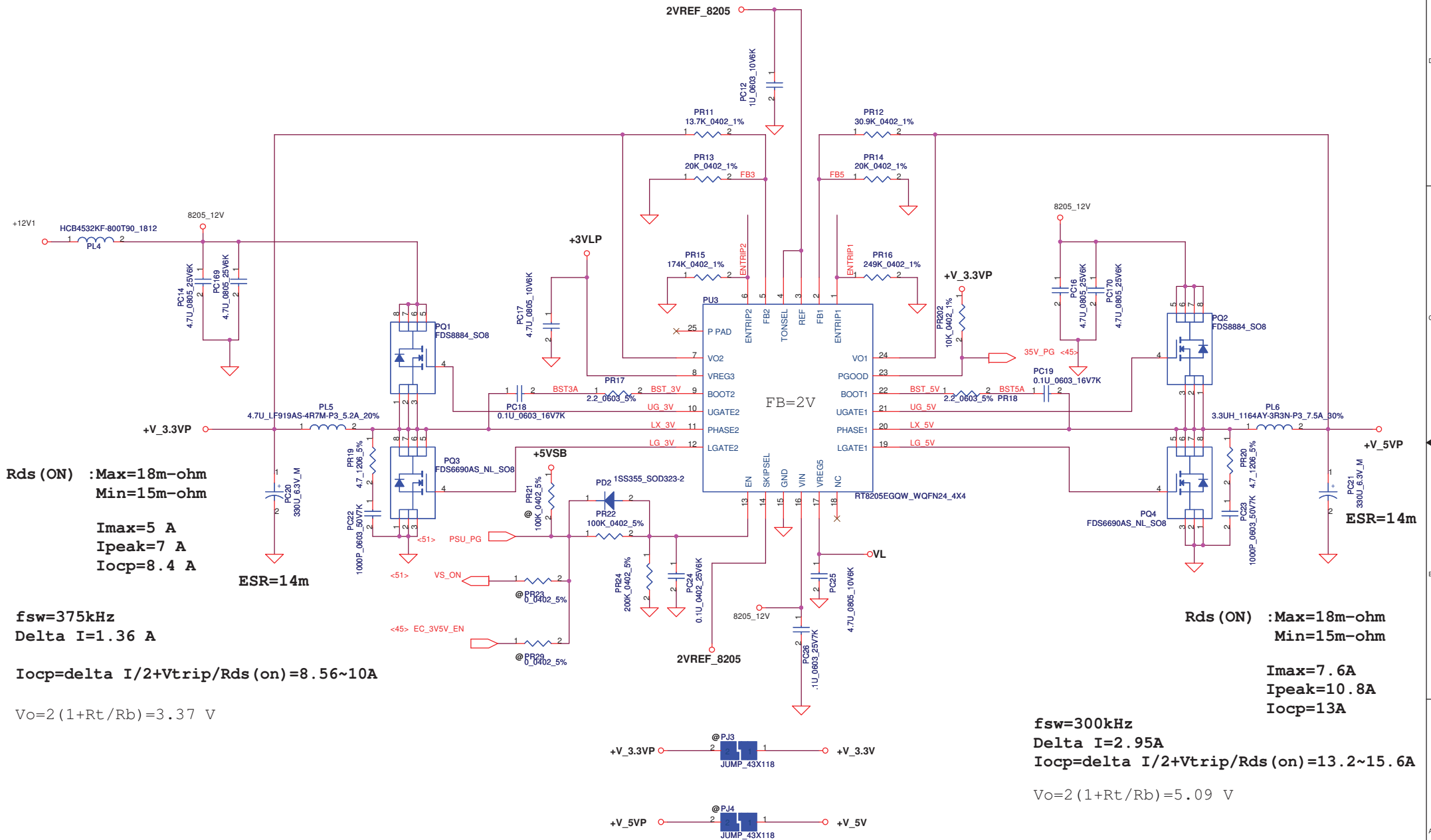
CPU thermal protection at 92 degree C  
Recovery at 57 degree C



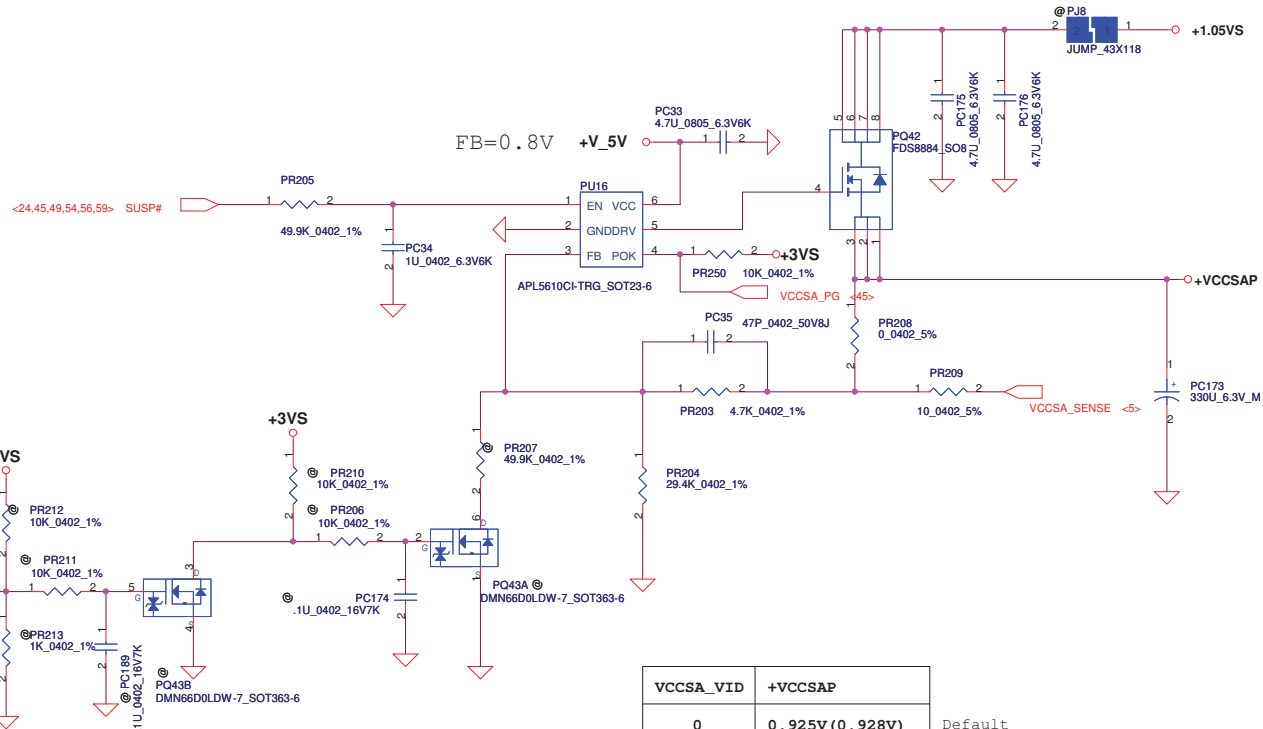
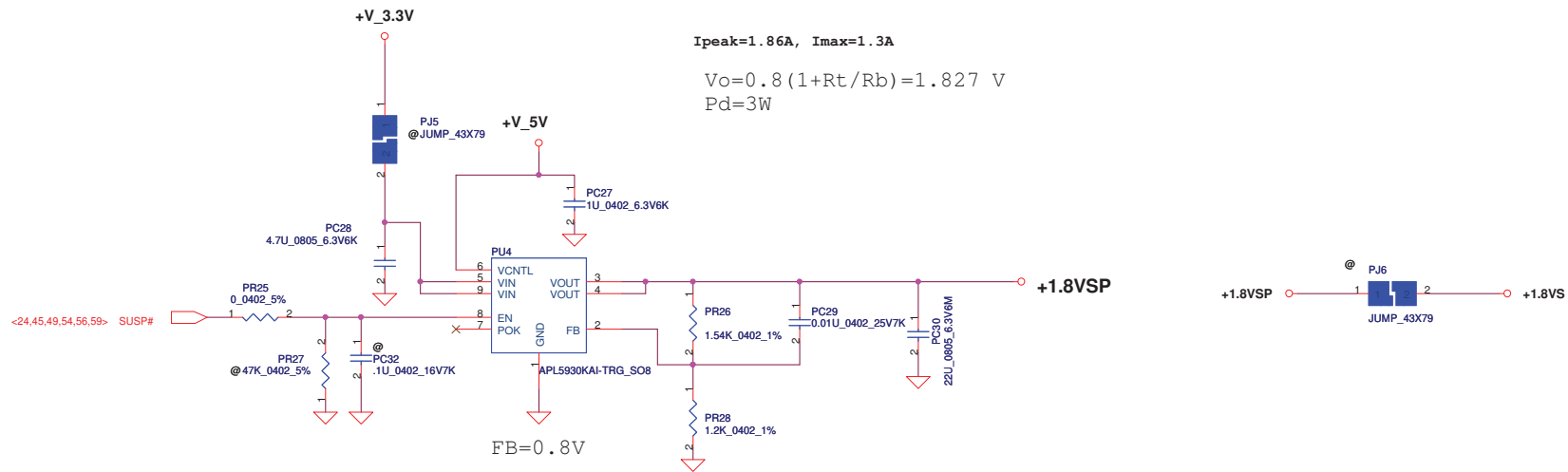
FOR EC suspend  
 $V_{FB} = 0.6V$   
 $V_o = V_{FB} * (1 + PR7/PR9) = 3.318V$   
 $I_{peak} = 0.062A, I_{max} = 0.045A$   
 Current limit >4A



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								Date:		Thursday, February 24, 2011		ISheet	



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Size	Document Number	0.1		Rev	
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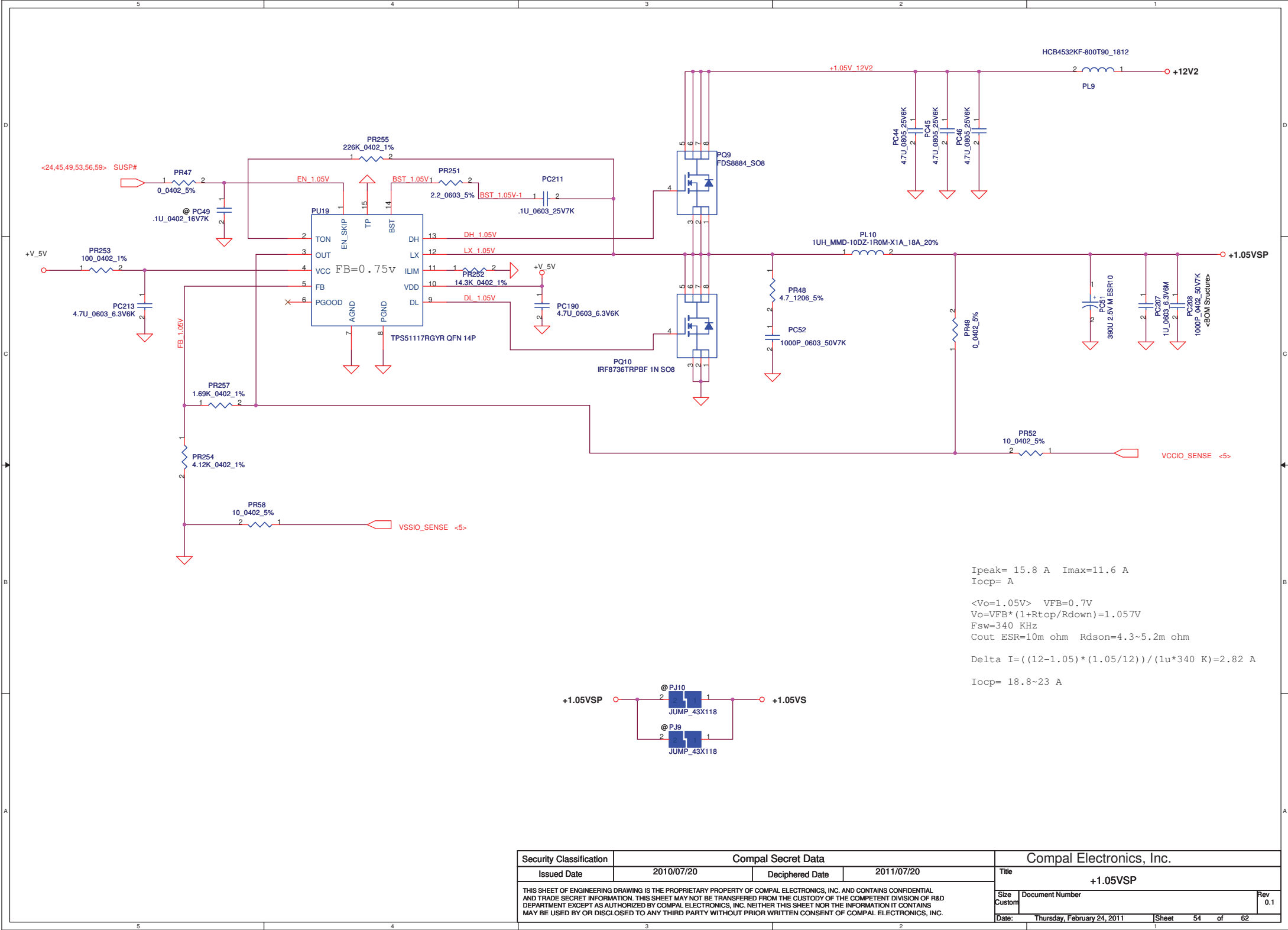


VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

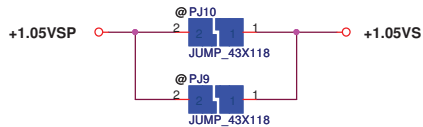
Default



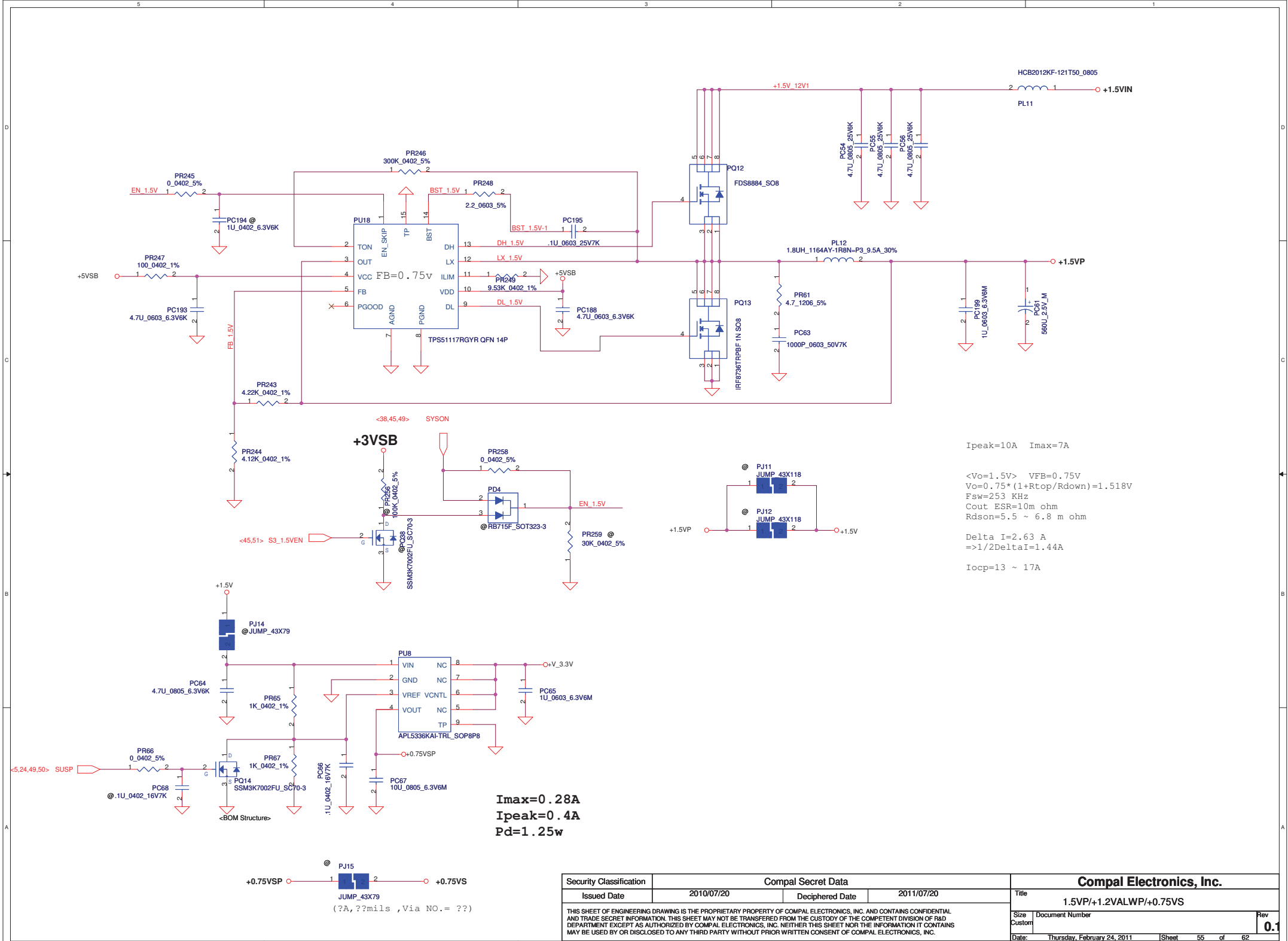
Security Classification				Compal Secret Data			Compal Electronics, Inc.		
Issued Date		2010/07/20		Deciphered Date		2011/07/20		Title	
								+VCCSA/+1.8VSP	
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Ipeak= 15.8 A Imax=11.6 A  
Iocp= A  
  
<Vo=1.05V> VFB=0.7V  
Vo=VFB\*(1+Rtop/Rdown)=1.057V  
Fsw=340 KHz  
Cout ESR=10m ohm Rdson=4.3~5.2m ohm  
  
Delta I=((12-1.05)\*(1.05/12))/(1u\*340 K)=2.82 A  
  
Iocp= 18.8~23 A



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Size Custom		Document Number		Rev 0.1	
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Ipeak=10A Imax=7A

<Vo=1.5V> VFB=0.75V  
Vo=0.75\*(1+Rtop/Rdown)=1.518V  
Fsw=253 KHz  
Cout ESR=10m ohm  
Rdson=5.5 ~ 6.8 m ohm

Delta I=2.63 A  
=>1/2DeltaI=1.44A

Iocp=13 ~ 17A

Imax=0.28A  
Ipeak=0.4A  
Pd=1.25w

(?A,??mils ,via NO.= ??)

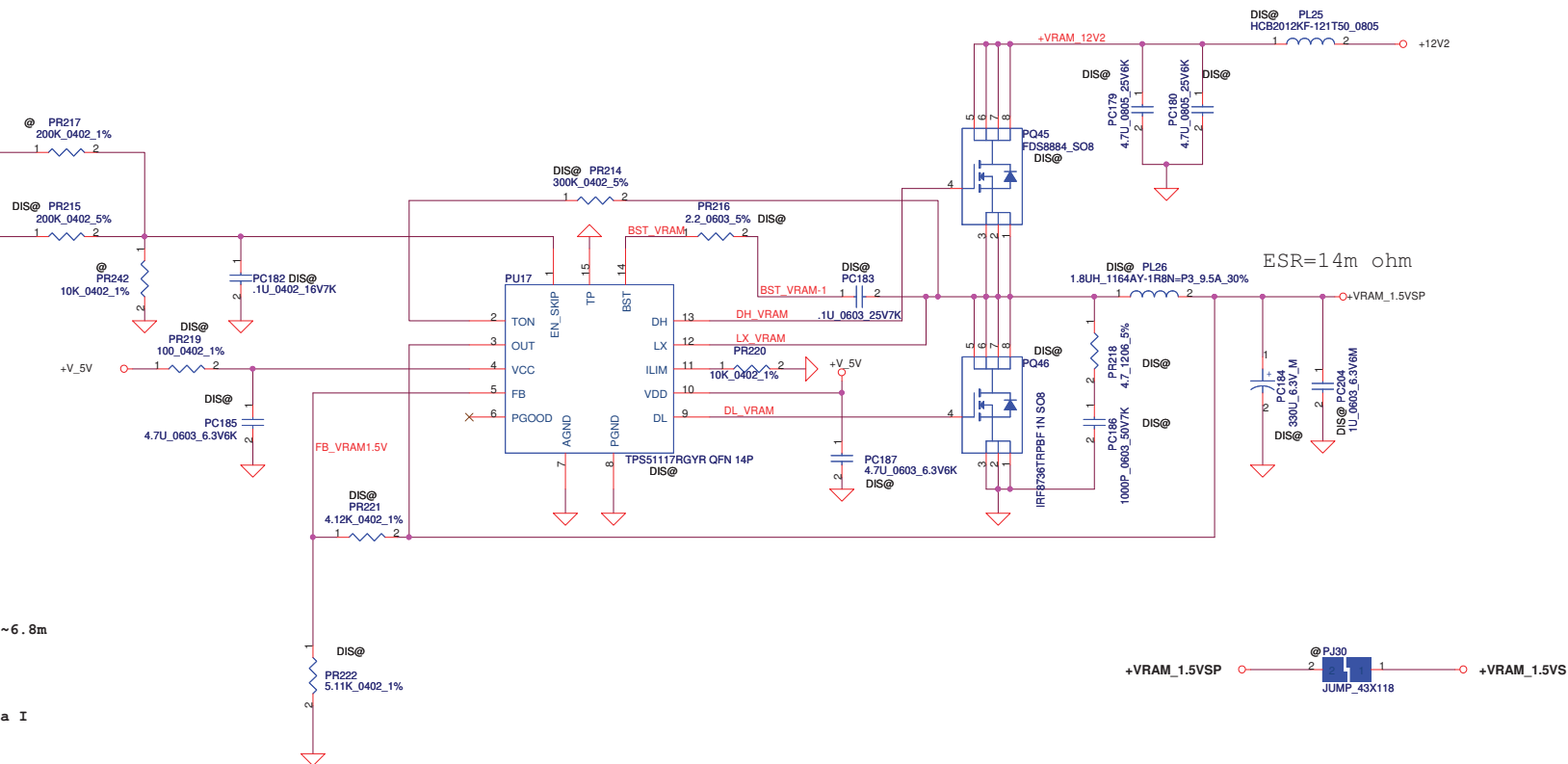
$I_p=10.2A$   $I_m=7A$

$<V_o=1.35V>$   $V_{FB}=0.75V$   
 $V_o=1.354V$   
 $F_{sw}=253\text{ KHz}$

$C_{out}\text{ ESR}=14m\text{ ohm}$   $R_{dson}=5.5\sim 6.8m$

$\Delta I=2.63\text{ A}$

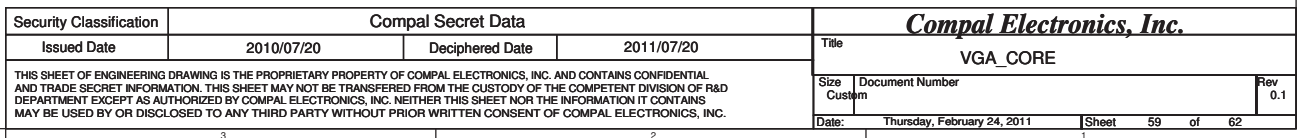
$V_{trip}=165mV$   
 $I_{ocp}=V_{trip}/(R_{dson})+1/2\Delta I$   
 $=16\text{ A}\sim 13\text{ A}$

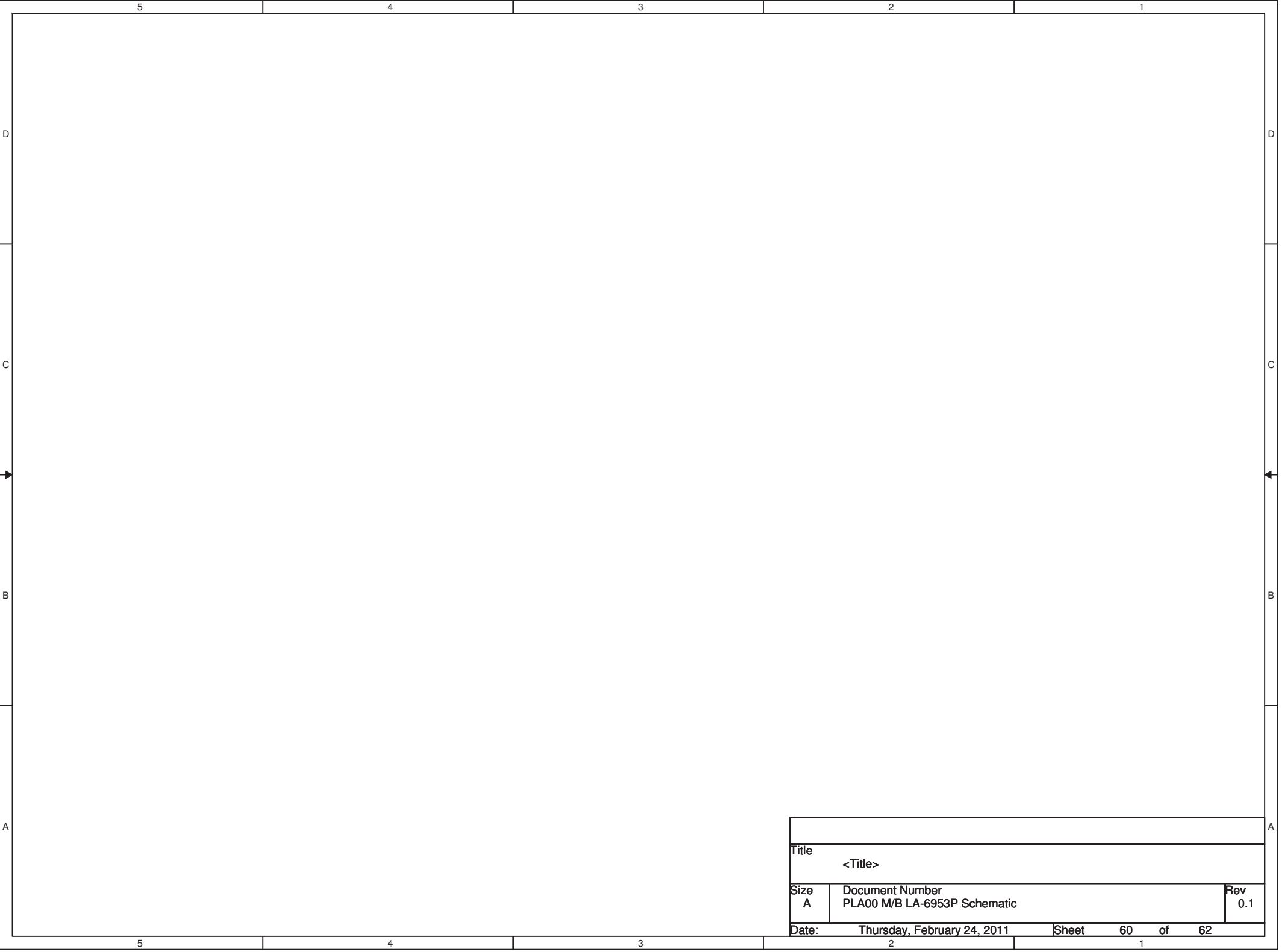


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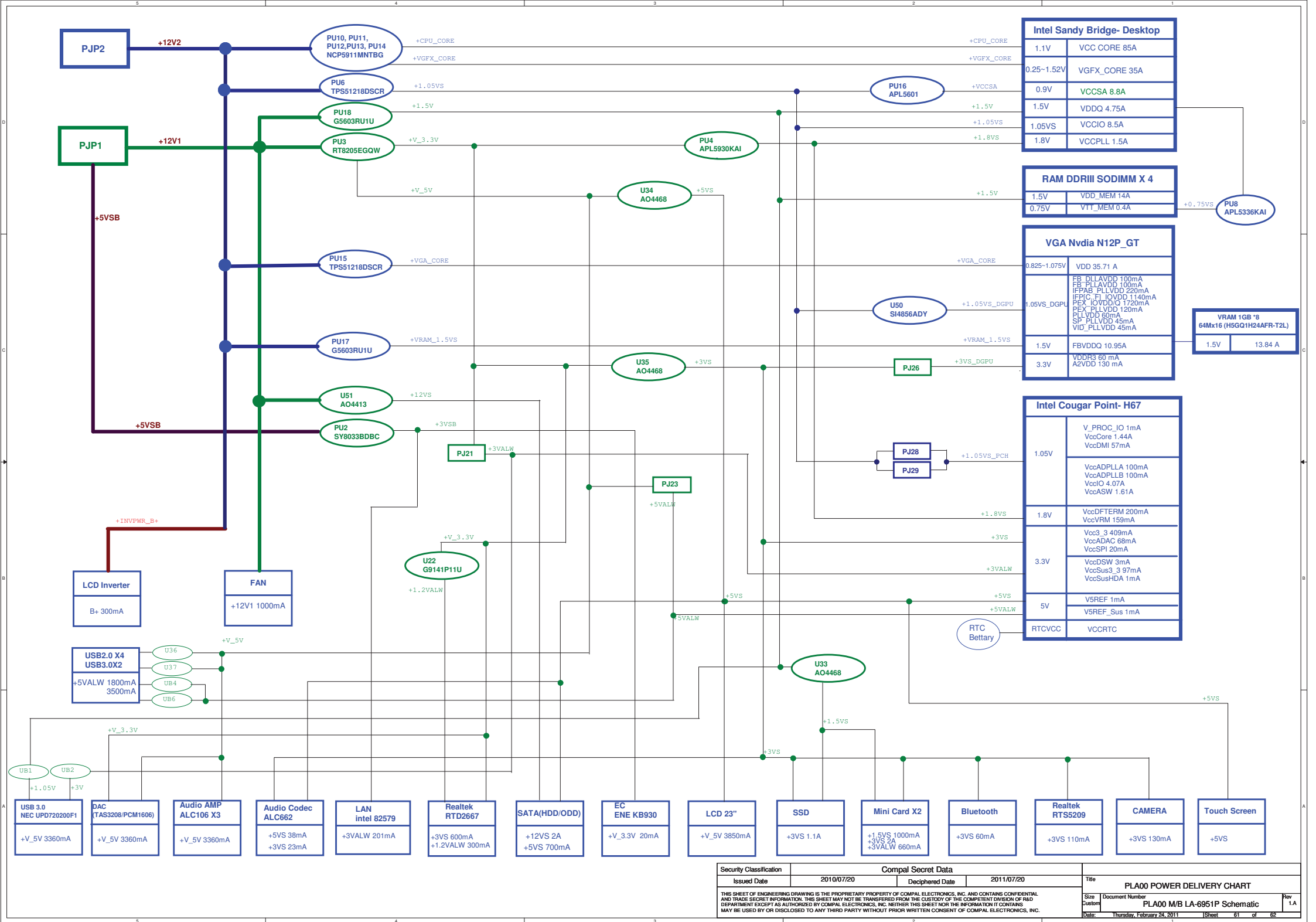








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Intel Sandy Bridge- Desktop	
1.1V	VCC CORE 85A
0.25~1.52V	VGFX_CORE 35A
0.9V	VCCSA 8.8A
1.5V	VDDQ 4.75A
1.05VS	VCCIO 8.5A
1.8V	VCCPLL 1.5A

RAM DDRIII SODIMM X 4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 0.4A

VGA Nvidia N12P_GT	
0.825~1.075V	VDD 35.71 A
1.05VS_DGPU	FB DLLAVDD 100mA FB PLLAVDD 100mA IFPAB PLLVDD 220mA IFPAB PLLVDD 1140mA PEX IOVDDIO 1720mA PEX PLLVDD 120mA PLVDD 60mA SP PLLVDD 45mA VID PLLVDD 45mA
1.5V	FBVDDQ 10.95A
3.3V	VDDR3 60 mA A2VDD 130 mA

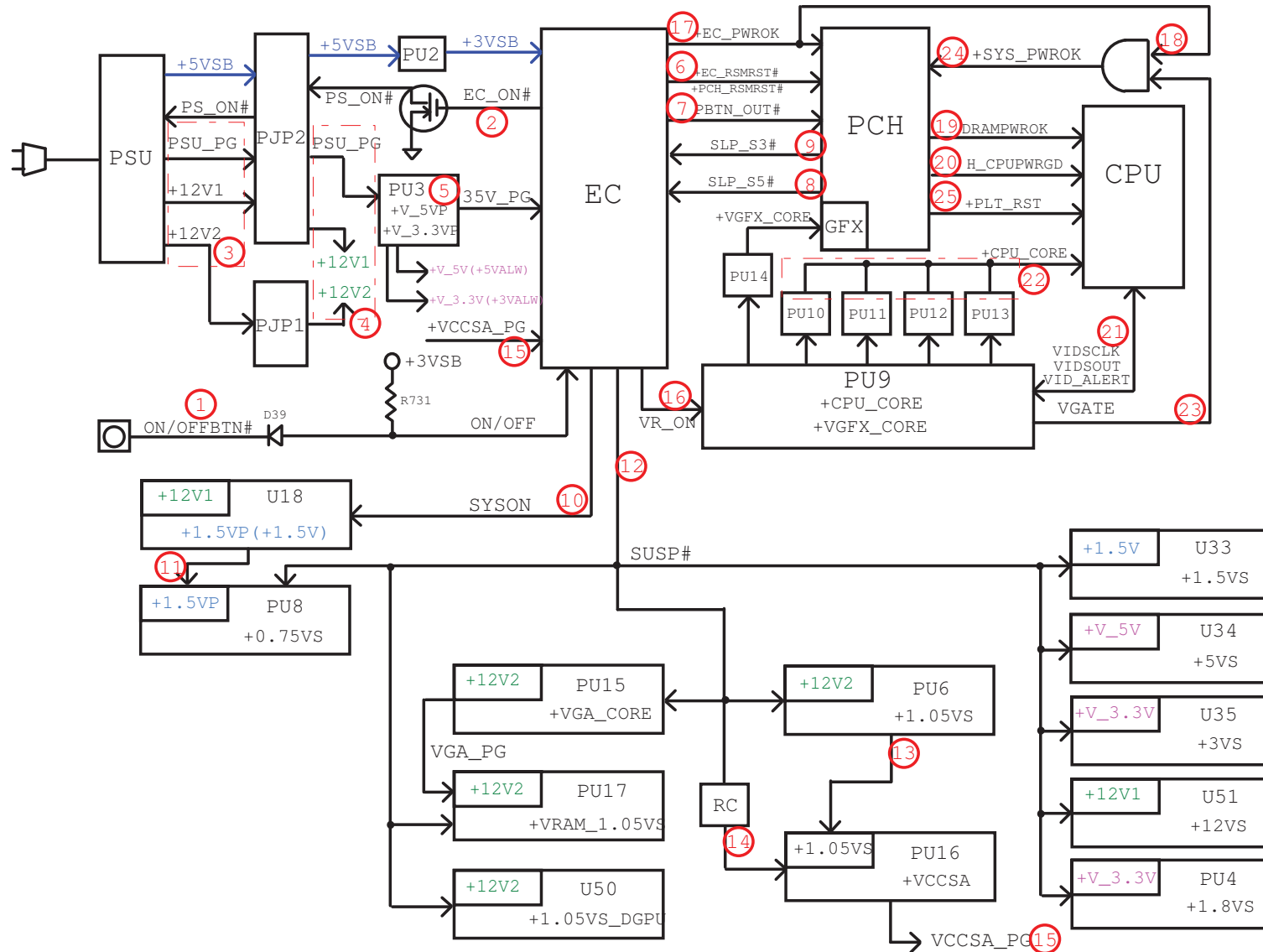
VRAM 1GB *8 64Mx16 (H5GQ1H24AFR-T2L)	
1.5V	13.84 A

Intel Cougar Point- H67	
1.05V	V_PROC_IO 1mA VccCore 1.44A VccDMI 57mA  VccADPLLA 100mA VccADPLLB 100mA VccIO 4.07A VccASW 1.61A
1.8V	VccDFTERM 200mA VccVRM 159mA
3.3V	Vcc3_3 409mA VccADAC 68mA VccSPI 20mA  VccDSW 3mA VccSus3_3 97mA VccSusHDA 1mA
5V	V5REF 1mA V5REF_Sus 1mA
RTCVCC	VCCRTC

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# COMPAL CONFIDENTIAL

**MODEL NAME:** *PLA00 Power Sequence Block Diagram (Discrete)*  
**PCB NAME:** *LA6951P*  
**REVISION:** *0.3*  
**DATE:** *2010/10/26*



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